MCP616/7/8/9
2.3V to 5.5V Micropower Bi-CMOS Op Amps

Features
- Low Input Offset Voltage: ±150 µV (maximum)
- Low Noise: 2.2 µVp-p (typical, 0.1 Hz to 10 Hz)
- Rail-to-Rail Output
- Low Input Offset Current: 0.3 nA (typical)
- Low Quiescent Current: 25 µA (maximum)
- Power Supply Voltage: 2.3V to 5.5V
- Unity Gain Stable
- Chip Select (CS) Capability: MCP618
- Industrial Temperature Range: -40°C to +85°C
- No Phase Reversal
- Available in Single, Dual and Quad Packages

Typical Applications
- Battery Power Instruments
- Weight Scales
- Strain Gauges
- Medical Instruments
- Test Equipment

Design Aids
- SPICE Macro Models
- Microchip Advanced Part Selector (MAPS)
- Mindi™ Circuit Designer & Simulator
- Analog Demonstration and Evaluation Boards
- Application Notes

Input Offset Voltage

Description
The MCP616/7/8/9 family of operational amplifiers (op amps) from Microchip Technology Inc. are capable of precision, low-power, single-supply operation. These op amps are unity-gain stable, have low input offset voltage (±150 µV, maximum), rail-to-rail output swing and low input offset current (0.3 nA, typical). These features make this family of op amps well suited for battery-powered applications.

The single MCP616, the single MCP618 with Chip Select (CS) and the dual MCP617 are all available in standard 8-lead PDIP, SOIC and MSOP packages. The quad MCP619 is offered in standard 14-lead PDIP, SOIC and TSSOP packages. All devices are fully specified from -40°C to +85°C, with power supplies from 2.3V to 5.5V.

Package Types

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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

- $V_{DD} - V_{SS}$ ........................................... 7.0V
- Current at Analog Input Pins ($V_{IN}^+$ and $V_{IN}^-$) ........... $\pm 2$ mA
- Analog Inputs ($V_{IN}^+$ and $V_{IN}^-$) †† † † .......................... $V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
- All other Inputs and Outputs ........................... $V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
- Difference Input Voltage .................................... $|V_{DD} - V_{SS}|$
- Output Short Circuit Current .......................... Continuous
- Current at Output and Supply Pins .................. $\pm 30$ mA
- Storage Temperature .................................... $-65°C$ to $+150°C$
- Maximum Junction Temperature ($T_J$) .................. $+150°C$
- ESD Protection On All Pins (HBM; MM) ................. $\geq 4$ kV; 400V

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† See Section 4.1.2 “Input Voltage and Current Limits”.

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, $V_{DD} = +2.3V$ to $+5.5V$, $V_{SS} = GND$, $T_A = +25°C$, $V_{CM} = V_{DD}/2$, $V_{OUT} = V_{DD}/2$ and $R_L = 100\, \Omega$ to $V_{DD}/2$.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
</table>
| Input Offset Voltage | $V_{OS}$ | -150 | — | +150 | µV | $T_A = -40°C$ to $+85°C$
| Power Supply Rejection | PSRR | 86 | 105 | — | dB | $V_{DD} = 5.0V$, $V_{CM} = 0.0V$ to $4.1V$
| Input Bias Current and Impedance | | | | |
| Input Bias Current | $I_B$ | -35 | -15 | -5 | nA | $T_A = -40°C$
| Input Offset Current | $I_{OS}$ | — | ±0.15 | — | nA | $T_A = +85°C$
| Common Mode Input Impedance | $Z_{CM}$ | — | 600|4 | — | MΩ|pF |
| Differential Input Impedance | $Z_{DIFF}$ | — | 3|2 | — | MΩ|pF |
| Common Mode Input Voltage Range | $V_{CMR}$ | $V_{SS}$ | $V_{DD} - 0.9$ | V | $V_{DD} = 5.0V$, $V_{CM} = 0.0V$ to $4.1V$
| Common Mode Rejection Ratio | CMRR | 80 | 100 | — | dB | $R_L = 25\, \Omega$ to $V_{DD}/2$, $V_{OUT} = V_{DD}/2$ to $0.05V$
| Open-Loop Gain | | | | |
| DC Open-Loop Gain (large signal) | $A_{OL}$ | 100 | 120 | — | dB | $R_L = 25\, \Omega$ to $V_{DD}/2$, $V_{OUT} = 0.05V$ to $V_{DD} - 0.05V$
| DC Open-Loop Gain (large signal) | $A_{OL}$ | 95 | 115 | — | dB | $R_L = 5\, \Omega$ to $V_{DD}/2$, $V_{OUT} = 0.1V$ to $V_{DD} - 0.1V$
| Output | | | | |
| Maximum Output Voltage Swing | $V_{OL}, V_{OH}$ | $V_{SS} + 15$ | — | $V_{DD} - 20$ | mV | $R_L = 25\, \Omega$ to $V_{DD}/2$, 0.5V input overdrive
| Linear Output Voltage Range | $V_{OUT}$ | $V_{SS} + 50$ | — | $V_{DD} - 50$ | mV | $R_L = 25\, \Omega$ to $V_{DD}/2$, 0.5V input overdrive
| Output Short Circuit Current | $I_{SC}$ | — | ±7 | — | mA | $V_{DD} = 2.3V$
| Power Supply | | | | |
| Supply Voltage | $V_{DD}$ | 2.3 | — | 5.5 | V | $I_{Q} = 0$
| Quiescent Current per Amplifier | $I_Q$ | 12 | 19 | 25 | µA | $V_{DD} = 5.5V$
AC ELECTRICAL CHARACTERISTICS

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain Bandwidth Product</td>
<td>GBWP</td>
<td>—</td>
<td>190</td>
<td>—</td>
<td>kHz</td>
<td></td>
</tr>
<tr>
<td>Phase Margin</td>
<td>PM</td>
<td>—</td>
<td>57</td>
<td>—</td>
<td>°</td>
<td>$G = +1V/V$</td>
</tr>
<tr>
<td>Slew Rate</td>
<td>SR</td>
<td>—</td>
<td>0.08</td>
<td>—</td>
<td>V/µs</td>
<td></td>
</tr>
</tbody>
</table>

**Noise**

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Noise Voltage</td>
<td>$E_{ni}$</td>
<td>—</td>
<td>2.2</td>
<td>—</td>
<td>µV$_{p-p}$</td>
<td>f = 0.1 Hz to 10 Hz</td>
</tr>
<tr>
<td>Input Noise Voltage Density</td>
<td>$e_{ni}$</td>
<td>—</td>
<td>32</td>
<td>—</td>
<td>nV/√Hz</td>
<td>f = 1 kHz</td>
</tr>
<tr>
<td>Input Noise Current Density</td>
<td>$i_{ni}$</td>
<td>—</td>
<td>70</td>
<td>—</td>
<td>fA/√Hz</td>
<td>f = 1 kHz</td>
</tr>
</tbody>
</table>

MCP618 CHIP SELECT (CS) ELECTRICAL CHARACTERISTICS

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>CS Logic Threshold, Low</td>
<td>$V_{IL}$</td>
<td>$V_{SS}$</td>
<td>—</td>
<td>0.2 $V_{DD}$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>CS Input Current, Low</td>
<td>$I_{CSL}$</td>
<td>—</td>
<td>0.01</td>
<td>—</td>
<td>µA $CS = V_{SS}$</td>
<td></td>
</tr>
<tr>
<td>CS Logic Threshold, High</td>
<td>$V_{IH}$</td>
<td>0.8 $V_{DD}$</td>
<td>—</td>
<td>$V_{DD}$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>CS Input Current, High</td>
<td>$I_{CSH}$</td>
<td>—</td>
<td>0.01</td>
<td>2</td>
<td>µA $CS = V_{DD}$</td>
<td></td>
</tr>
<tr>
<td>GND Current</td>
<td>$I_{SS}$</td>
<td>-2</td>
<td>-0.05</td>
<td>—</td>
<td>µA $CS = V_{DD}$</td>
<td></td>
</tr>
<tr>
<td>Amplifier Output Leakage</td>
<td>$I_{O(LEAK)}$</td>
<td>—</td>
<td>10</td>
<td>—</td>
<td>nA $CS = V_{DD}$</td>
<td></td>
</tr>
</tbody>
</table>

**CS Dynamic Specifications**

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>CS Low to Amplifier Output Turn-on Time</td>
<td>$I_{ON}$</td>
<td>—</td>
<td>9</td>
<td>100</td>
<td>µs $CS = 0.2V_{DD}$ to $V_{OUT} = 0.9V_{DD}/2$, $G = +1V/V$, $R_{L} = 1kΩ$ to $V_{SS}$</td>
<td></td>
</tr>
<tr>
<td>CS High to Amplifier Output High-Z</td>
<td>$I_{OFF}$</td>
<td>—</td>
<td>0.1</td>
<td>—</td>
<td>µs $CS = 0.8V_{DD}$ to $V_{OUT} = 0.1V_{DD}/2$, $G = +1V/V$, $R_{L} = 1kΩ$ to $V_{SS}$</td>
<td></td>
</tr>
</tbody>
</table>

**CS Hysteresis**

$V_{HYST}$ — 0.6 — V $V_{DD} = 5.0V$

**FIGURE 1-1:** Timing Diagram for the CS Pin on the MCP618.
TEMPERATURE CHARACTERISTICS

**Electrical Specifications:** Unless otherwise indicated, \( V_{DD} = +2.3\text{V} \) to +5.5V and \( V_{SS} = \text{GND} \).

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Specified Temperature Range</td>
<td>( T_A )</td>
<td>-40</td>
<td>—</td>
<td>+85</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>( T_A )</td>
<td>-40</td>
<td>—</td>
<td>+125</td>
<td>°C</td>
<td>Note 1</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>( T_A )</td>
<td>-65</td>
<td>—</td>
<td>+150</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

**Thermal Package Resistances**

<table>
<thead>
<tr>
<th>Package Type</th>
<th>( \theta_{JA} )</th>
<th>—</th>
<th>211</th>
<th>—</th>
<th>°C/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal Resistance, 8L-MSOP</td>
<td>( \theta_{JA} )</td>
<td>—</td>
<td>89.3</td>
<td>—</td>
<td>°C/W</td>
</tr>
<tr>
<td>Thermal Resistance, 8L-PDIP</td>
<td>( \theta_{JA} )</td>
<td>—</td>
<td>149.5</td>
<td>—</td>
<td>°C/W</td>
</tr>
<tr>
<td>Thermal Resistance, 14L-PDIP</td>
<td>( \theta_{JA} )</td>
<td>—</td>
<td>70</td>
<td>—</td>
<td>°C/W</td>
</tr>
<tr>
<td>Thermal Resistance, 14L-SOIC</td>
<td>( \theta_{JA} )</td>
<td>—</td>
<td>95.3</td>
<td>—</td>
<td>°C/W</td>
</tr>
<tr>
<td>Thermal Resistance, 14L-TSSOP</td>
<td>( \theta_{JA} )</td>
<td>—</td>
<td>100</td>
<td>—</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

**Note 1:** The MCP616/7/8/9 operate over this extended temperature range, but with reduced performance. In any case, the Junction Temperature (\( T_J \)) must not exceed the Absolute Maximum specification of +150°C.

### 1.1 Test Circuits

The test circuits used for the DC and AC tests are shown in Figure 1-2 and Figure 1-3. The bypass capacitors are laid out according to the rules discussed in Section 4.6 “Supply Bypass”.

**FIGURE 1-2:** AC and DC Test Circuit for Most Non-Inverting Gain Conditions.

**FIGURE 1-3:** AC and DC Test Circuit for Most Inverting Gain Conditions.
2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

**Note:** Unless otherwise indicated, $V_{DD} = +2.3\text{V}$ to $+5.5\text{V}$, $V_{SS} = \text{GND}$, $T_A = +25\text{°C}$, $V_{CM} = V_{DD}/2$, $V_{OUT} = V_{DD}/2$, $R_L = 100\ \Omega$ to $V_{DD}/2$ and $C_L = 60\ \text{pF}$.

**FIGURE 2-1:** Input Offset Voltage at $V_{DD} = 5.5\text{V}$.

**FIGURE 2-2:** Input Offset Voltage at $V_{DD} = 2.3\text{V}$.

**FIGURE 2-3:** Input Bias Current at $V_{DD} = 5.5\text{V}$.

**FIGURE 2-4:** Input Offset Voltage Drift at $V_{DD} = 5.5\text{V}$.

**FIGURE 2-5:** Input Offset Voltage Drift at $V_{DD} = 2.3\text{V}$.

**FIGURE 2-6:** Input Offset Current at $V_{DD} = 5.5\text{V}$.
Note: Unless otherwise indicated, V_{DD} = +2.3V to +5.5V, V_{SS} = GND, T_A = 25°C, V_{CM} = V_{DD}/2, V_{OUT} \approx V_{DD}/2, R_L = 100 \, k\Omega \text{ to } V_{DD}/2 \text{ and } C_L = 60 \, pF.

**FIGURE 2-7:** Input Offset Voltage vs. Ambient Temperature.

**FIGURE 2-8:** Quiescent Current vs. Ambient Temperature.

**FIGURE 2-9:** Maximum Output Voltage Swing vs. Ambient Temperature at $R_L = 5 \, k\Omega$

**FIGURE 2-10:** Input Bias, Offset Currents vs. Ambient Temperature.

**FIGURE 2-11:** CMRR, PSRR vs. Ambient Temperature.

**FIGURE 2-12:** Maximum Output Voltage Swing vs. Ambient Temperature at $R_L = 25 \, k\Omega$
Note: Unless otherwise indicated, \( V_{DD} = +2.3\text{V to } +5.5\text{V}, V_{SS} = \text{GND}, T_A = 25^\circ\text{C}, V_{CM} = V_{DD}/2, V_{OUT} \approx V_{DD}/2, R_L = 100\text{ k}\Omega \) to \( V_{DD}/2 \) and \( C_L = 60\text{ pF}. \)

**FIGURE 2-13:** Output Short Circuit Current vs. Ambient Temperature.

**FIGURE 2-14:** Slew Rate vs. Ambient Temperature.

**FIGURE 2-15:** Input Bias, Offset Currents vs. Common Mode Input Voltage.

**FIGURE 2-16:** Gain Bandwidth Product, Phase Margin vs. Ambient Temperature.

**FIGURE 2-17:** Input Offset Voltage vs. Common Mode Input Voltage.

**FIGURE 2-18:** Input Offset Voltage vs. Output Voltage.
Note: Unless otherwise indicated, $V_{DD} = +2.3\,\text{V}$ to $+5.5\,\text{V}$, $V_{SS} = \text{GND}$, $T_A = 25^\circ\text{C}$, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $R_L = 100\,\text{k}\Omega$ to $V_{DD}/2$ and $C_L = 60\,\text{pF}$.

**FIGURE 2-19:** Quiescent Current vs. Power Supply Voltage.

**FIGURE 2-20:** DC Open-Loop Gain vs. Load Resistance.

**FIGURE 2-21:** Gain-Bandwidth Product, Phase Margin vs. Load Resistance.

**FIGURE 2-22:** Output Voltage Headroom vs. Output Current Magnitude.

**FIGURE 2-23:** DC Open-Loop Gain vs. Power Supply Voltage.

**FIGURE 2-24:** Channel-to-Channel Separation vs. Frequency (MCP617 and MCP619 only).
Note: Unless otherwise indicated, $V_{DD} = +2.3\text{V}$ to $+5.5\text{V}$, $V_{SS} = \text{GND}$, $T_A = 25^\circ\text{C}$, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $R_L = 100 \text{k}\Omega$ to $V_{DD}/2$ and $C_L = 60 \text{pF}$.

**FIGURE 2-25:** Open-Loop Gain, Phase vs. Frequency.

**FIGURE 2-26:** Input Noise Voltage, Current Densities vs. Frequency.

**FIGURE 2-27:** Small-Signal, Non-Inverting Pulse Response.

**FIGURE 2-28:** CMRR, PSRR vs. Frequency.

**FIGURE 2-29:** Maximum Output Voltage Swing vs. Frequency.

**FIGURE 2-30:** Small-Signal, Inverting Pulse Response.
Note: Unless otherwise indicated, $V_{DD} = +2.3\text{V to } +5.5\text{V}$, $V_{SS} = \text{GND}$, $T_A = 25^\circ\text{C}$, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $R_L = 100\ \text{k}\Omega$ to $V_{DD}/2$ and $C_L = 60\ \text{pF}$.

**FIGURE 2-31:** Large-Signal, Non-Inverting Pulse Response.

**FIGURE 2-32:** Chip Select (CS) to Amplifier Output Response Time (MCP618 only).

**FIGURE 2-33:** The MCP616/7/8/9 Show No Phase Reversal.

**FIGURE 2-34:** Large-Signal, Inverting Pulse Response.

**FIGURE 2-35:** Chip Select (CS) Internal Hysteresis (MCP618 only).

**FIGURE 2-36:** Measured Input Current vs. Input Voltage (below $V_{SS}$).
3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1.

### TABLE 3-1: PIN FUNCTION TABLE

<table>
<thead>
<tr>
<th>MCP616</th>
<th>MCP617</th>
<th>MCP618</th>
<th>MCP619</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSOP, PDIP, SOIC</td>
<td>MSOP, PDIP, SOIC</td>
<td>MSOP, PDIP, SOIC</td>
<td>PDIP, SOIC, TSSOP</td>
</tr>
<tr>
<td>Symbol</td>
<td>Description</td>
<td></td>
<td></td>
</tr>
<tr>
<td>--------</td>
<td>-------------</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6 V OUT, VOUTA</td>
<td>Output (op amp A)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2 V IN- VINA-</td>
<td>Inverting Input (op amp A)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3 V IN+, VINA+</td>
<td>Non-inverting Input (op amp A)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7 VDD</td>
<td>Positive Power Supply</td>
<td></td>
<td></td>
</tr>
<tr>
<td>— 5 V INB+</td>
<td>Non-inverting Input (op amp B)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>— 6 V INB-</td>
<td>Inverting Input (op amp B)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>— 7 VOUTB</td>
<td>Output (op amp B)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>— 8 VOUTC</td>
<td>Output (op amp B)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>— 9 V INC-</td>
<td>Inverting Input (op amp C)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>— 10 V INC+</td>
<td>Non-inverting Input (op amp C)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4 VSS</td>
<td>Negative Power Supply</td>
<td></td>
<td></td>
</tr>
<tr>
<td>— 12 V IND+</td>
<td>Non-inverting Input (op amp D)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>— 13 V IND-</td>
<td>Inverting Input (op amp D)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>— 14 VOUTD</td>
<td>Output (op amp D)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>— 8 CS</td>
<td>Chip Select</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1, 5, 8 NC</td>
<td>No Internal Connection</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

3.1 Analog Outputs

The output pins are low-impedance voltage sources.

3.2 Analog Inputs

The non-inverting and inverting inputs are high-impedance PNP inputs with low bias currents.

3.3 Chip Select Digital Input (CS)

This is a CMOS, Schmitt-triggered input that places the MCP618 op amp into a low-power mode of operation.

3.4 Power Supply Pins (VDD, VSS)

The positive power supply (VDD) is 2.3V to 5.5V higher than the negative power supply (VSS). For normal operation, the other pins are at voltages between VSS and VDD.

Typically, these parts are used in a single-supply (positive) supply configuration. In this case, VSS is connected to ground and VDD is connected to the supply. VDD will need bypass capacitors.
4.0 APPLICATIONS INFORMATION

The MCP616/7/8/9 family of op amps is manufactured using Microchip’s state-of-the-art CMOS process, which includes PNP transistors. These op amps are unity-gain stable and suitable for a wide range of general purpose applications.

4.1 Rail-to-Rail Inputs

4.1.1 PHASE REVERSAL

The MCP616/7/8/9 op amp is designed to prevent phase reversal when the input pins exceed the supply voltages. Figure 2-36 shows the input voltage exceeding the supply voltage without any phase reversal.

4.1.2 INPUT VOLTAGE AND CURRENT LIMITS

The ESD protection on the inputs can be depicted as shown in Figure 4-1. This structure was chosen to protect the input transistors, and to minimize input bias current (Ib). The input ESD diodes clamp the inputs when they try to go more than one diode drop below VSS. They also clamp any voltages that go too far above VDD; their breakdown voltage is high enough to allow normal operation, and low enough to bypass quick ESD events within the specified limits.

In order to prevent damage and/or improper operation of these op amps, the circuit they are in must limit the currents and voltages at the VIN+ and VIN− pins (see “Absolute Maximum Ratings” at the beginning of Section 1.0 “Electrical Characteristics”). Figure 4-2 shows the recommended approach to protecting these inputs. The internal ESD diodes prevent the input pins (VIN+ and VIN−) from going too far below ground, and the resistors R1 and R2 limit the possible current drawn out of the input pins. Diodes D1 and D2 prevent the input pins (VIN+ and VIN−) from going too far above VDD, and dump any currents onto VDD. When implemented as shown, resistors R1 and R2 also limit the current through D1 and D2.

4.1.3 NORMAL OPERATION

The inputs of the MCP616/7/8/9 op amps connect to a differential PNP input stage. The common mode input voltage range (VCMR) includes ground in single-supply systems (VSS), but does not include VDD. This means that the amplifier input behaves linearly as long as the common mode input voltage (VCM) is kept within the specified VCMR limits (VSS to VDD−0.9V at +25°C).

4.2 DC Offsets

The MCP616/7/8/9 family of op amps have a PNP input differential pair that gives good DC performance. They have very low input offset voltage (±150 nV, maximum) at TA = +25°C, with a typical bias current of -15 nA (sourced out of the inputs).

There must be a DC path to ground (or power supply) from both inputs, or the op amp will not bias properly. The DC resistances seen by the op amp inputs (R1||R2 and R4||RS in Figure 4-3) need to be equal and less than 100 kΩ, to minimize the total DC offset.

FIGURE 4-1: Simplified Analog Input ESD Structures.
FIGURE 4-3: Example Circuit for Calculating DC Offset.

To calculate the DC bias point and DC offset, convert the circuit to its DC equivalent:

- Replace capacitors with open circuits
- Replace inductors with short circuits
- Replace AC voltage sources with short circuits
- Replace AC current sources with open circuits
- Convert DC sources and resistances into their Thevenin equivalent form

The DC equivalent circuit for Figure 4-3 is shown in Figure 4-4.

FIGURE 4-4: Equivalent DC Circuit.

Now calculate the nominal DC bias point with offset:

\[
G_N = \frac{1}{R_2 / R_1}
\]

\[
V_{OOS} = G_N \left[ V_{OS} + I_B \left( (R_1 || R_2) - R_{EQ} \right) - I_{OS} \left( (R_1 || R_2) + R_{EQ} \right) / 2 \right]
\]

\[
V_{CM} = V_{EQ} - \frac{(I_B + I_{OS}/2) \cdot R_{EQ}}{R_{EQ}}
\]

\[
V_{OUT} = V_{EQ} \left( G_N \right) - V_1 \left( (G_N - 1) + V_{OOS} \right)
\]

Where:

- \( G_N \) = op amp’s noise gain (from the non-inverting input to the output)
- \( V_{OOS} \) = circuit’s output offset voltage
- \( V_{OS} \) = op amp’s input offset voltage
- \( I_B \) = op amp’s input bias current
- \( I_{OS} \) = op amp’s input offset current
- \( V_{CM} \) = op amp’s common mode input voltage

Use the worst-case specs and source values to determine the worst-case output voltage range and offset for your design. Make sure the common mode input voltage range and output voltage range are not exceeded.

4.3 Rail-to-Rail Output

There are two specifications that describe the output swing capability of the MCP616/7/8/9 family of op amps. The first specification (Maximum Output Voltage Swing) defines the absolute maximum swing that can be achieved under the specified load conditions. For instance, the output voltage swings to within 15 mV of the negative rail with a 25 kΩ load tied to \( V_{DD}/2 \). Figure 2-33 shows how the output voltage is limited when the input goes beyond the linear region of operation.

The second specification that describes the output swing capability of these amplifiers is the Linear Output Voltage Range. This specification defines the maximum output swing that can be achieved while the amplifier still operates in its linear region. To verify linear operation in this range, the large-signal DC Open-Loop Gain \( (A_{OL}) \) is measured at points inside the supply rails. The measurement must meet the specified \( A_{OL} \) conditions in the specification table.
4.4 Capacitive Loads

Driving large capacitive loads can cause stability problems for voltage feedback op amps. As the load capacitance increases, the feedback loop’s phase margin decreases and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in the step response. A unity-gain buffer (G = +1) is the most sensitive to capacitive loads, though all gains show the same general behavior.

When driving large capacitive loads with these op amps (e.g., > 60 pF when G = +1), a small series resistor at the output (R\text{ISO} in Figure 4-5) improves the feedback loop’s phase margin (stability) by making the output load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitive load.

**FIGURE 4-5:** Output Resistor; R\text{ISO} stabilizes large capacitive loads.

Figure 4-6 gives recommended R\text{ISO} values for different capacitive loads and gains. The x-axis is the normalized load capacitance (C\text{L}/G\text{N}), where G\text{N} is the circuit’s noise gain. For non-inverting gains, G\text{N} and the Signal Gain are equal. For inverting gains, G\text{N} is 1+|Signal Gain| (e.g., -1 V/V gives G\text{N} = +2 V/V).

**FIGURE 4-6:** Recommended R\text{ISO} Values for Capacitive Loads.

After selecting R\text{ISO} for your circuit, double-check the resulting frequency response peaking and step response overshoot. Modify R\text{ISO}’s value until the response is reasonable. Bench evaluation and simulations with the MCP616/7/8/9 SPICE macro model are helpful.

4.5 MCP618 Chip Select (\overline{CS})

The MCP618 is a single op amp with Chip Select (\overline{CS}). When \overline{CS} is pulled high, the supply current drops to 50 nA (typical) and flows through the \overline{CS} pin to V\text{SS}. When this happens, the amplifier output is put into a high-impedance state. By pulling \overline{CS} low, the amplifier is enabled. The \overline{CS} pin has an internal 5 M\Omega (typical) pull-down resistor connected to V\text{SS}, so it will go low if the \overline{CS} pins is left floating. Figure 1-1 shows the output voltage and supply current response to a \overline{CS} pulse.

4.6 Supply Bypass

With this family of operational amplifiers, the power supply pin (V\text{DD} for single supply) should have a local bypass capacitor (i.e., 0.01 µF to 0.1 µF) within 2 mm for good high-frequency performance. It may use a bulk capacitor (i.e., 1 µF or larger) within 100 mm to provide large, slow currents. This bulk capacitor is not required and can be shared with other analog parts.

4.7 Unused Op Amps

An unused op amp in a quad package (MCP619) should be configured as shown in Figure 4-7. These circuits prevent the output from toggling and causing crosstalk. Circuits A sets the op amp at its minimum noise gain. The resistor divider produces any desired reference voltage within the output voltage range of the op amp; the op amp buffers that reference voltage. Circuit B uses the minimum number of components and operates as a comparator, but it may draw more current.

**FIGURE 4-7:** Unused Op Amps.
4.8 PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\,\Omega$. A 5V difference would cause 5 pA of current to flow, which is greater than the MCP616/7/8/9 family’s bias current at 25°C (1 pA, typical).

The easiest way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example is shown below in Figure 4-8.

![Guard Ring Layout](image_url)

**FIGURE 4-8:** Example Guard Ring Layout for Inverting Gain.

1. Non-inverting Gain and Unity Gain Buffer:
   a) Connect the non-inverting pin ($V_{IN^+}$) to the input with a wire that does not touch the PCB surface.
   b) Connect the guard ring to the inverting input pin ($V_{IN^-}$). This biases the guard ring to the common mode input voltage.

2. Inverting Gain and Transimpedance gain (convert current to voltage, such as photo detectors) amplifiers:
   a) Connect the guard ring to the non-inverting input pin ($V_{IN^+}$). This biases the guard ring to the same reference voltage as the op amp (e.g., $V_{DD}/2$ or ground).
   b) Connect the inverting pin ($V_{IN^-}$) to the input with a wire that does not touch the PCB surface.

4.9 Application Circuits

4.9.1 HIGH GAIN PRE-AMPLIFIER

The MCP616/7/8/9 op amps are well suited to amplifying small signals produced by low-impedance sources/sensors. The low offset voltage, low offset current and low noise fit well in this role. Figure 4-9 shows a typical pre-amplifier connected to a low-impedance source ($V_S$ and $R_S$).

![High Gain Pre-amplifier](image_url)

**FIGURE 4-9:** High Gain Pre-amplifier.

For the best noise and offset performance, the source resistance $R_S$ needs to be less than 15 kΩ. The DC resistances at the inputs are equal to minimize the offset voltage caused by the input bias currents (Section 4.2 “DC Offsets”). In this circuit, the DC gain is 10 V/V, which will give a typical bandwidth of 19 kHz.

4.9.2 TWO OP AMP INSTRUMENTATION AMPLIFIER

The two-op amp instrumentation amplifier shown in Figure 4-10 serves the function of taking the difference of two input voltages, level-shifting it and gaining it to the output. This configuration is best suited for higher gains (i.e., gain > 3 V/V). The reference voltage ($V_{REF}$) is typically at mid-supply ($V_{DD}/2$) in a single-supply environment.

![Two-Op Amp Instrumentation Amplifier](image_url)

**FIGURE 4-10:** Two-Op Amp Instrumentation Amplifier.

The key specifications that make the MCP616/7/8/9 family appropriate for this application circuit are low input bias current, low offset voltage and high common-mode rejection.
4.9.3 THREE OP AMP INSTRUMENTATION AMPLIFIER

A classic, three-op amp instrumentation amplifier is illustrated in Figure 4-11. The two-input op amps provide differential signal gain and a common mode gain of +1. The output op amp is a difference amplifier, which converts its input signal from differential to a single-ended output; it rejects common mode signals at its input. The gain of this circuit is simply adjusted with one resistor (R<sub>G</sub>). The reference voltage (V<sub>REF</sub>) is typically referenced to mid-supply (V<sub>DD/2</sub>) in single-supply applications.

![Figure 4-11: Three-Op Amp Instrumentation Amplifier.](image)

\[
V_{OUT} = (V_1 - V_2) \left(1 + \frac{2R_2}{R_G}\right) \left(\frac{R_4}{R_3}\right) + V_{REF}
\]

4.9.4 PRECISION GAIN WITH GOOD LOAD ISOLATION

In Figure 4-12, the MCP616 op amp, R<sub>1</sub> and R<sub>2</sub> provide a high gain to the input signal (V<sub>IN</sub>). The MCP616’s low offset voltage makes this an accurate circuit.

The MCP606 is configured as a unity-gain buffer. It isolates the MCP616’s output from the load, increasing the high gain stage’s precision. Since the MCP606 has a higher output current, and the two amplifiers are housed in separate packages, there is minimal change in the MCP616’s offset voltage due to loading effect.

![Figure 4-12: Precision Gain with Good Load Isolation.](image)

\[
V_{OUT} = V_{IN}(1 + \frac{R_2}{R_1})
\]
5.0 DESIGN AIDS

Microchip provides the basic design tools needed for the MCP616/7/8/9 family of op amps.

5.1 SPICE Macro Model

The latest SPICE macro model for the MCP616/7/8/9 op amps is available on the Microchip web site at www.microchip.com. This model is intended to be an initial design tool that works well in the op amp's linear region of operation over the temperature range. See the model file for information on its capabilities.

Bench testing is a very important part of any design and cannot be replaced with simulations. Also, simulation results using this macro model need to be validated by comparing them to the data sheet specifications and characteristic curves.

5.2 Mindi™ Circuit Designer & Simulator

Microchip's Mindi™ Circuit Designer & Simulator aids in the design of various circuits useful for active filter, amplifier and power-management applications. It is a free online circuit designer & simulator available from the Microchip web site at www.microchip.com/mindi. This interactive circuit designer & simulator enables designers to quickly generate circuit diagrams, simulate circuits. Circuits developed using the Mindi Circuit Designer & Simulator can be downloaded to a personal computer or workstation.

5.3 Microchip Advanced Part Selector (MAPS)

MAPS is a software tool that helps semiconductor professionals efficiently identify Microchip devices that fit a particular design requirement. Available at no cost from the Microchip website at www.microchip.com/maps, the MAPS is an overall selection tool for Microchip’s product portfolio that includes Analog, Memory, MCUs and DSCs. Using this tool you can define a filter to sort features for a parametric search of devices and export side-by-side technical comparison reports. Helpful links are also provided for Datasheets, Purchase, and Sampling of Microchip parts.

5.4 Analog Demonstration and Evaluation Boards

Microchip offers a broad spectrum of Analog Demonstration and Evaluation Boards that are designed to help you achieve faster time to market. For a complete listing of these boards and their corresponding user’s guides and technical information, visit the Microchip web site at www.microchip.com/analogtools.

Two of our boards that are especially useful are:
  • P/N SOIC8EV: 8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board
  • P/N SOIC14EV: 14-Pin SOIC/TSSOP/DIP Evaluation Board

5.5 Application Notes

The following Microchip Application Notes are available on the Microchip web site at www.microchip.com/appnotes and are recommended as supplemental reference resources.

ADN003: “Select the Right Operational Amplifier for your Filtering Circuits”, DS21821
AN722: “Operational Amplifier Topologies and DC Specifications”, DS00722
AN723: “Operational Amplifier AC Specifications and Applications”, DS00723
AN884: “Driving Capacitive Loads With Op Amps”, DS00884
AN990: “Analog Sensor Conditioning Circuits – An Overview”, DS00990

These application notes and others are listed in the design guide:
“Signal Chain Design Guide”, DS21825
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

Legend:

XX...X Customer-specific information
Y Year code (last digit of calendar year)
YY Year code (last 2 digits of calendar year)
WW Week code (week of January 1 is week ‘01’)
NNN Alphanumeric traceability code
Pb-free JEDEC designator for Matte Tin (Sn)
* This package is Pb-free. The Pb-free JEDEC designator (*3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.
Package Marking Information (Continued)

14-Lead PDIP (300 mil) (MCP619) Examples:

```
XXXXXXXXXXXXXXXX
XXXXXXXXXXXXXXXX
0812256
```

OR

```
XXYYWWNNN
```

14-Lead SOIC (150 mil) (MCP619) Examples:

```
XXXXXXXXXXXX
XXXXXXXXXXXX
0812256
```

OR

```
YYWWNNN
```

14-Lead TSSOP (MCP619) Example:

```
YYYYWW
0812
```

```
619IST
0812
256
```
8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

![8-Lead Plastic Micro Small Outline Package (MS) [MSOP]](image)

### Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.
   - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   - REF: Reference Dimension, usually without tolerance, for information purposes only.

### Table: Dimension Limits

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Microchip Technology Drawing C04-111B
8-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

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Notes:
1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” per side.
4. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-018B
8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

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Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B
8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

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**RECOMMENDED LAND PATTERN**

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Notes:
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A
14-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

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**Notes:**
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2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-005B
### 14-Lead Plastic Small Outline (SL) – Narrow, 3.90 mm Body [SOIC]

#### Note:
For the most current package drawings, please see the Microchip Packaging Specification located at [http://www.microchip.com/packaging](http://www.microchip.com/packaging)

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<tr>
<td>Mold Draft Angle Bottom</td>
<td>β</td>
<td>5°</td>
<td>–</td>
<td>15°</td>
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#### Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.
   
   **BSC:** Basic Dimension. Theoretically exact value shown without tolerances.
   **REF:** Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-065B
14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

RECOMMENDED LAND PATTERN

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<td>Distance Between Pads</td>
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Notes:
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2065A
14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

### Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

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Microchip Technology Drawing C04-087B
APPENDIX A: REVISION HISTORY

Revision C (October 2008)
The following is the list of modifications:
1. Added Section 1.1 “Test Circuits”.
2. Added Figure 2-36.
3. Added Section 4.1.1 “Phase Reversal”, Section 4.1.2 “Input Voltage and Current Limits”, and Section 4.1.3 “Normal Operation”.
4. Updated Figure 4-7.
5. Updated Section 5.0 “Design Aids”.
6. Updated Section 6.0 “Packaging Information”.

Revision B (April 2005)
The following is the list of modifications:
1. Clarified specifications found in Section 1.0 “Electrical Characteristics”.
2. Updated Section 2.0 “Typical Performance Curves” and added input noise current density plot.
3. Added Section 3.0 “Pin Descriptions”.
4. Updated Section 4.0 “Applications Information”.
5. Updated the SPICE macro model and added information on the FilterLab software, in Section 5.0 “Design Aids”.
6. Corrected package marking information (Section 6.0 “Packaging Information”).
7. Added Appendix A: “Revision History”.

Revision A (April 2001)
• Original Release of this Document.
# PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

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<tr>
<td>/XX</td>
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</table>

Device:
- MCP616: Single Operational Amplifier
- MCP616T: Single Operational Amplifier (Tape and Reel for SOIC, MSOP)
- MCP617: Dual Operational Amplifier
- MCP617T: Dual Operational Amplifier (Tape and Reel for SOIC and MSOP)
- MCP618: Single Operational Amplifier w/Chip Select (CS)
- MCP618T: Single Operational Amplifier w/Chip Select (CS) (Tape and Reel for SOIC and MSOP)
- MCP619: Quad Operational Amplifier
- MCP619T: Quad Operational Amplifier (Tape and Reel for SOIC and TSSOP)

Temperature Range: I = -40°C to +85°C

Package:
- MS = Plastic MSOP, 8-lead
- P = Plastic DIP (300mil Body), 8-lead, 14-lead
- SN = Plastic SOIC (3.90 mm body), 8-lead
- SL = Plastic SOIC (3.90 mm Body), 14-lead (MCP619)
- ST = Plastic TSSOP (4.4mm Body), 14-lead (MCP619)

Examples:

a) MCP616-I/P: Industrial Temperature, 8 lead PDIP.
b) MCP616-I/SN: Industrial Temperature, 8 lead SOIC.
c) MCP616T-I/MS: Tape and Reel, Industrial Temperature, 8 lead MSOP.

a) MCP617-I/MS: Industrial Temperature, 8 lead MSOP.
b) MCP617T-I/MS: Tape and Reel, Industrial Temperature, 8 lead MSOP.
c) MCP617-I/P: Industrial Temperature, 8 lead PDIP.

a) MCP618-I/SN: Industrial Temperature, 8 lead SOIC.
b) MCP618T-I/SN: Tape and Reel, Industrial Temperature, 8 lead SOIC.
c) MCP618-I/P: Industrial Temperature, 8 lead PDIP.

a) MCP619T-I/SL: Tape and Reel, Industrial Temperature, 14 lead SOIC.
b) MCP619T-I/ST: Tape and Reel, Industrial Temperature, 14 lead TSSOP.
c) MCP619-I/P: Industrial Temperature, 14 lead PDIP.
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