Features

- Fast read access time 55ns
- Low-power CMOS operation
 - 100µA max standby
 - 40mA max active at 5MHz
- JEDEC standard packages
 - 40-lead PDIP
 - 44-lead PLCC
- Direct upgrade from 512Kbit, 1Mbit, and 2Mbit Atmel[®] AT27C516, AT27C1024, and AT27C2048) EPROMs
- 5V ± 10% supply
- High-reliability CMOS technology
 - 2,000V ESD protection
 - 200mA latchup immunity
- Rapid programming algorithm 50µs/word (typical)
- CMOS- and TTL-compatible inputs and outputs
- Integrated product identification code
- Industrial temperature range
- Green (Pb/halide-free) packaging option

1. Description

The Atmel AT27C4096 is a low-power, high-performance, 4,194,304-bit, one-time programmable, read-only memory (OTP EPROM) organized as 256K by 16 bits. It requires a single 5V power supply in normal read mode operation. Any word can be accessed in less than 55ns, eliminating the need for speed reducing WAIT states. The x16 organization makes this part ideal for high-performance, 16- and 32-bit microprocessor systems.

In read mode, the AT27C4096 typically consumes 15mA. Standby mode supply current is typically less than 10μ A.

The AT27C4096 is available in industry-standard, JEDEC-approved, one-time programmable (OTP) PDIP and PLCC packages. The device features two-line control ($\overline{\text{CE}}$, $\overline{\text{OE}}$) to eliminate bus contention in high speed systems.

With high-density 256K word storage capability, the AT27C4096 allows firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

The AT27C4096 has additional features that ensure high quality and efficient production use. The rapid programming algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 50µs/word. The Integrated product identification code electronically identifies the device and manufacturer. This feature is used by industry-standard programming equipment to select the proper programming algorithms and voltages.



4Mb (256K x 16) One-time Programmable, Read-only Memory

Atmel AT27C4096

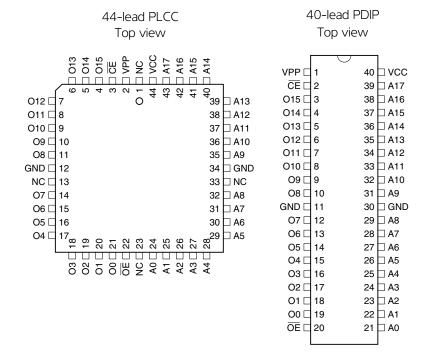




2. Pin configurations

Pin name	Function
A0 - A17	Addresses
00 - 015	Outputs
CE	Chip enable
ŌĒ	Output enable
NC	No connect

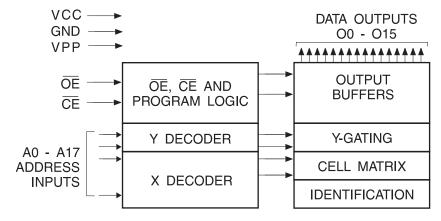
Note: Both GND pins must be connected



3. System considerations

Switching between active and standby conditions via the chip enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed datasheet limits, resulting in device nonconformance. At a minimum, a $0.1\mu\text{F}$, high-frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the V_{CC} and ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a $4.7\mu\text{F}$ bulk electrolytic capacitor should be utilized, again connected between the V_{CC} and ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

Figure 3-1. Block diagram



4. Absolute maximum ratings*

Temperature under bias55°C to +125°C
Storage temperature65°C to +150°C
Voltage on any pin with respect to ground2.0V to +7.0V ⁽¹⁾
Voltage on A9 with respect to ground2.0V to +14.0V ⁽¹⁾
V _{PP} supply voltage with respect to ground2.0V to +14.0V ⁽¹⁾

*NOTICE: Stresses beyond those listed under "Absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended

periods may affect device reliability.

Note: 1. Maximum voltage is -0.6V DC, which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is $V_{CC} + 0.75V$ DC, which may overshoot to +7.0V for pulses of less than 20ns.

5. DC and AC characterisitcs

Table 5-1. Operating modes

Mode/Pin	CE	ŌĒ	Ai	V_{PP}	Outputs
Read	V _{IL}	V _{IL}	Ai	X ⁽¹⁾	D _{OUT}
Output disable	X	V _{IH}	X	X	High Z
Standby	V _{IH}	×	X	X ⁽⁵⁾	High Z
Rapid program ⁽²⁾	V _{IL}	V _{IH}	Ai	V_{PP}	D _{IN}
PGM verify	V _{IH}	V _{IL}	Ai	V_{PP}	D _{OUT}
PGM inhibit	V _{IH}	V _{IH}	X	V_{PP}	High Z
Product identification ⁽⁴⁾	$V_{ m lL}$	V _{IL}	$A9 = V_{H}^{(3)}$ $A0 = V_{IH} \text{ or } V_{IL}$ $A1 - A17 = V_{IL}$	V _{CC}	Identification code

Notes:

- X can be V_{II} or V_{IH}.
- 2. Refer to the Programming characteristics.
- 3. $V_H = 12.0 \pm 0.5 V$.
- 4. Two identifier words may be selected. All Ai inputs are held low (V_{IL}) , except A9, which is set to V_{H} , and A0, which is toggled low (V_{IL}) to select the manufacturer's identification word and high (V_{IH}) to select the device code word.
- 5. Standby V_{CC} current (I_{SB}) is specified with $V_{PP} = V_{CC}$. $V_{CC} > V_{PP}$ will cause a slight increase in I_{SB} .

Table 5-2. DC and AC operating conditions for read operation

	Atmel AT	27C4096
	-55	-90
Industrial operating temperature (case)	-40°C - 85°C	-40°C - 85°C
V _{CC} power supply	5V ± 10%	5V ± 10%





Table 5-3. DC and operating characteristics for read operation

Symbol	Parameter	Condition	Min	Max	Units
ILI	Input load current	$V_{IN} = OV \text{ to } V_{CC}$		± 1	μΑ
I _{LO}	Output leakage current	$V_{OUT} = 0V \text{ to } V_{CC}$		± 5	μΑ
I _{PP1} ⁽²⁾	V _{PP} ⁽¹⁾ read/standby current	$V_{PP} = V_{CC}$		10	μΑ
	V (1) standby a weat	I_{SB1} (CMOS) $\overline{CE} = V_{CC} \pm 0.3V$		100	μΑ
I _{SB}	V _{CC} ⁽¹⁾ standby current	I_{SB2} (TTL) \overline{CE} = 2.0 to V_{CC} + 0.5V		1	mA
I _{CC}	V _{CC} active current	$f = 5MHz$, $I_{OUT} = 0mA$, $\overline{CE} = V_{IL}$		40	mΑ
V _{IL}	Input low voltage		-0.6	0.8	V
V _{IH}	Input high voltage		2.0	V _{CC} + 0.5	V
V _{OL}	Output low voltage	I _{OL} = 2.1mA		0.4	V
V _{OH}	Output high voltage	I _{OH} = -400μA	2.4		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} , and removed simultaneously with or after V_{PP} .

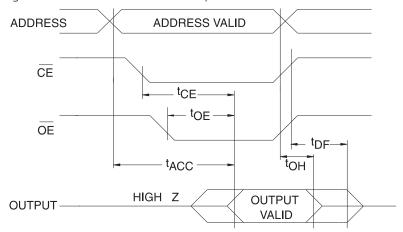
Table 5-4. AC characteristics for read operation

			Atmel AT27C4096				
			-:	55	1	90	
Symbol	Parameter	Condition	Min	Max	Min	Max	Units
t _{ACC} ⁽¹⁾	Address to output delay	$\overline{CE} = \overline{OE} = V_{IL}$		55		90	ns
t _{CE} ⁽¹⁾	CE to output delay	$\overline{OE} = V_{IL}$		55		90	ns
t _{OE} ⁽¹⁾	OE to output delay	CE = V _{IL}		20		35	ns
t _{DF} ⁽¹⁾	OE or CE high to output float, whichever occurred first			20		20	ns
t _{OH} ⁽¹⁾	Output hold from address, $\overline{\text{CE}}$ or $\overline{\text{OE}}$, whichever occurred first		7		0		ns

Note: 1. See the AC waveforms for read operation diagram.

^{2.} V_{PP} may be connected directly to V_{CC} , except during programming. The supply current would then be the sum of I_{CC} and I_{PP} .

Figure 5-1. AC waveforms for read operation⁽¹⁾

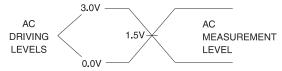


Notes:

- 1. Timing measurement references are 0.8V and 2.0V. Input AC drive levels are 0.45V and 2.4V, unless otherwise specified.
- 2. $\overline{\text{OE}}$ may be delayed up to t_{CE} t_{OE} after the falling edge of $\overline{\text{CE}}$ without impact on t_{CE} .
- 3. $\overline{\text{OE}}$ may be delayed up to t_{ACC} t_{OE} after the address is valid without impact on t_{ACC}
- 4. This parameter is only sampled, and is not 100% tested.
- 5. Output float is defined as the point when data is no longer driven.

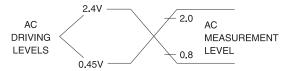
Figure 5-2. Input test waveforms and measurement levels

For -55 devices only:



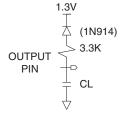
 t_R , t_F < 5ns (10% to 90%)

For -90 devices:



 t_R , t_F < 20ns (10% to 90%)

Figure 5-3. Output test load



Note: CL = 100pF including jig capacitance.



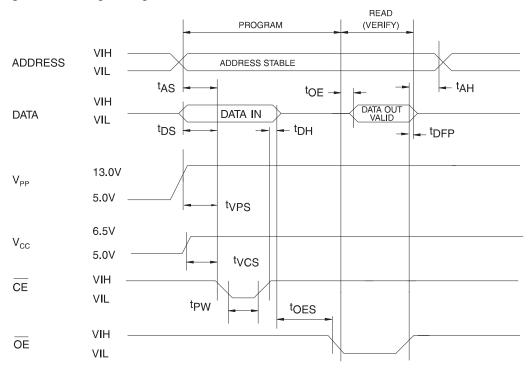


Table 5-5. Pin capacitance f = 1MHz, $T = 25^{\circ}C^{(1)}$

Symbol	Тур	Max	Units	Conditions
C _{IN}	4	10	pF	V _{IN} = 0V
C _{OUT}	8	12	pF	V _{OUT} = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled, and is not 100% tested.

Figure 5-4. Programming waveforms⁽¹⁾



Notes:

- 1. The input timing reference is 0.8V for $\rm V_{IL}$ and 2.0V for $\rm V_{IH}$
- 2. t_{OE} and t_{DFP} are characteristics of the device, but must be accommodated by the programmer.
- 3. When programming the Atmel AT27C4096, a $0.1\mu F$ capacitor is required across V_{pp} and ground to suppress spurious voltage transients.

Table 5-6. DC programming characteristics

$$T_A = 25 \pm 5$$
°C, $V_{CC} = 6.5 \pm 0.25$ V, $V_{PP} = 13.0 \pm 0.25$ V

			Limits		
Symbol	Parameter	Test conditions	Min	Max	Units
ILI	Input load current	$V_{IN} = V_{IL}, V_{IH}$		±10	μΑ
V _{IL}	Input low level		-0.6	0.8	V
V _{IH}	Input high level		2.0	V _{CC} + 0.7	V
V _{OL}	Output low voltage	I _{OL} = 2.1mA		0.4	V
V _{OH}	Output high voltage	Ι _{ΟΗ} = -400μΑ	2.4		V
I _{CC2}	V _{CC} supply current (program and verify)			50	mA
I _{PP2}	V _{PP} supply current	$\overline{CE} = V_{IL}$		30	mA
V _{ID}	A9 product identification voltage		11.5	12.5	V

Table 5-7. AC programming characteristics

$$T_A = 25 \pm 5$$
°C, $V_{CC} = 6.5 \pm 0.25$ V, $V_{pp} = 13.0 \pm 0.25$ V

			Lin	nits	
Symbol	Parameter	Test conditions ⁽¹⁾	Min	Max	Units
t _{AS}	Address setup time		2		μs
t _{OES}	OE setup time		2		μs
t _{DS}	Data setup time	Input rise and fall times : (10% to 90%) 20ns	2		μs
t _{AH}	Address hold time	(10/0 to 30/0) 20113	0		μs
t _{DH}	Data hold time	Input pulse levels	2		μs
t _{DFP}	OE high to output float delay ⁽²⁾	0.45V to 2.4V	0	130	ns
t _{VPS}	V _{PP} setup time	Input timing reference level:	2		μs
t _{VCS}	V _{CC} setup time	0.8V to 2.0V	2		μs
t _{PW}	CE program pulse width ⁽³⁾		47.5	52.5	μs
t _{OE}	Data valid from OE	Output timing reference level 0.8V to 2.0V		150	ns
t _{PRT}	V _{PP} pulse rise time during programming		50		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously with or after V_{PP} .

- 2. This parameter is only sampled, and is not 100% tested. Output float is defined as the point where data is no longer driven. See timing diagram.
- 3. Program pulse width tolerance is $50\mu s \pm 5\%$.

Table 5-8. The Atmel AT27C4096 intergrated product identification code

		Pins									
Codes	A0	015-08	07	O6	O5	04	О3	02	01	00	Hex data
Manufacturer	0	0	0	0	0	1	1	1	1	0	001E
Device type	1	0	1	1	1	1	0	1	0	0	00F4

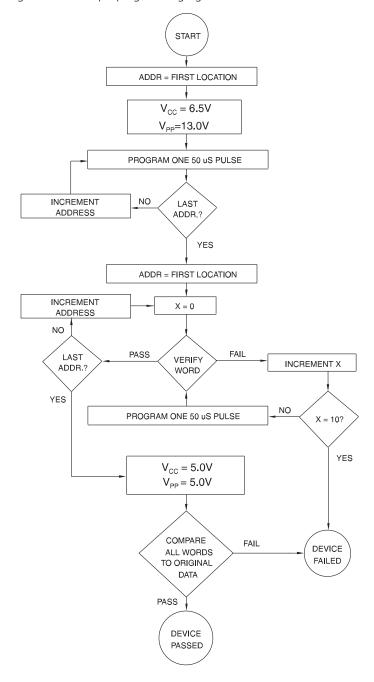




6. Rapid programming algorithm

A 50 μ s $\overline{\text{CE}}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and V_{PP} is raised to 13.0V. Each address is first programmed with one 50 μ s $\overline{\text{CE}}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a word fails to pass verification, up to 10 successive 50 μ s pulses are applied with a verification after each pulse. If the word fails to verify after 10 pulses have been applied, the part is considered failed. After the word verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0V and V_{CC} to 5.0V. All words are read again and compared with the original data to determine if the device passes or fails.

Figure 6-1. Rapid programming algorithm



7. Ordering information

Green Package (Pb/halide-free)

	I _{CC} (mA)					
t _{ACC} (ns)	Active	Standby	Atmel ordering code	Package	Lead finish	Operation range
55	40	0.1	AT27C4096-55JU	44J	Matte tin	Industrial (-40°C to 85°C)
90	40	0.1	AT27C4096-90JU AT27C4096-90PU	44J 40P6	Matte tin	Industrial (-40°C to 85°C)

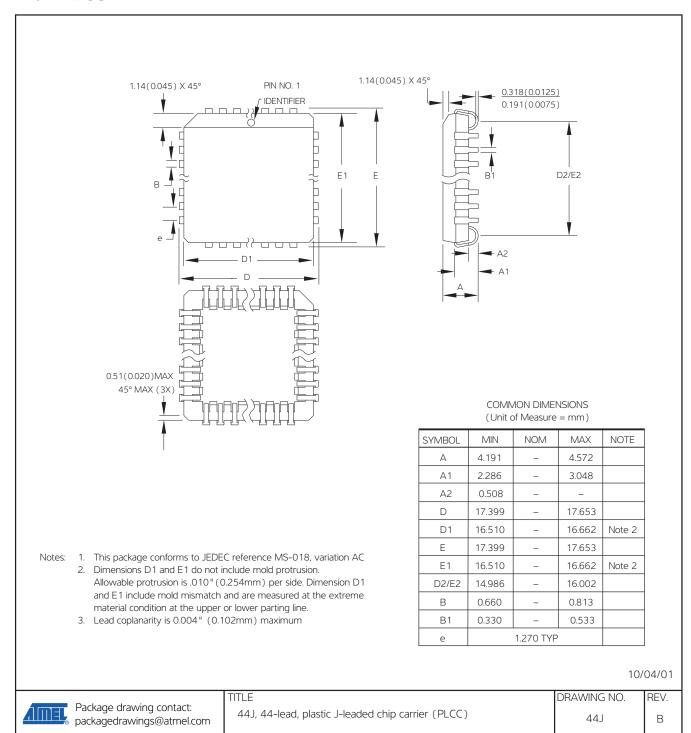
	Package type		
44J	44J 44-lead, plastic, J-leaded chip carrier (PLCC)		
40P6	40P6 40-lead, 0.600 " wide, plastic, dual inline package (PDIP)		



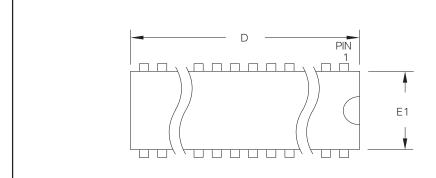


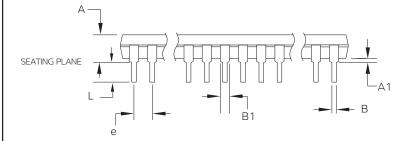
8. Packaging information

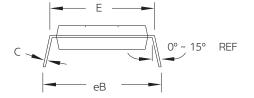
44J – PLCC



40P6 - PDIP







1. This package conforms to JEDEC reference MS-011, variation AC

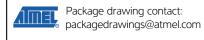
2. Dimensions D and E1 do not include mold flash or protrusion. mold flash or protrusion shall not exceed 0.25mm (0.010").

COMMON DIMENSIONS (Unit of Measure = mm)

(
SYMBOL	MIN	NOM	MAX	NOTE
А	_	_	4.826	
A1	0.381	_	_	
D	52.070	_	52.578	Note 2
Е	15.240	_	15.875	
E1	13.462	_	13.970	Note 2
В	0.356	-	0.559	
B1	1.041	_	1.651	
L	3.048	_	3.556	
С	0.203	-	0.381	
eB	15.494	_	17.526	
е	2.540 TYP			

09/28/01

В



TITLE 40P6, 40-lead (0.600"/15.24mm wide) Plastic dual inline package (PDIP) $\,$ DRAWING NO. REV. 40P6





9. Revision history

Doc. rev.	Date	Comments	
0311J	04/2011	Remove VSOP package Add lead finish to ordering information	
0311	12/2007	Add teld in ish to ordering information	



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