

P-Channel Power MOSFET

-30V, -3A, 60mΩ

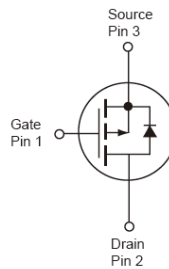
Features

- Advance Trench Process Technology
- High Density Cell Design for Ultra Low On-resistance
- Pb-free plating
- RoHS compliant
- Halogen-free package

Application

- Load Switch
- PA Switch

KEY PERFORMANCE PARAMETERS			
PARAMETER		VALUE	UNIT
V_{DS}		-30	V
$R_{DS(on)}$ (max)	$V_{GS} = -10V$	60	mΩ
	$V_{GS} = -4.5V$	90	
Q_g		9.52	nC



P-Channel MOSFET

Notes: Moisture sensitivity level: level 3. Per J-STD-020

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current ^(Note 1)	$T_A = 25^\circ C$	I_D	-3	A
Pulsed Drain Current ^(Note 2)		I_{DM}	-10	A
Continuous Source Current (Diode Conduction)		I_S	-1.9	A
Total Power Dissipation	$T_A = 25^\circ C$	P_{TOT}	1.25	W
	$T_A = 70^\circ C$		0.8	
Operating Junction and Storage Temperature Range		T_J, T_{STG}	- 55 to +150	$^\circ C$

THERMAL PERFORMANCE			
PARAMETER	SYMBOL	LIMIT	UNIT
Junction to Case Thermal Resistance	$R_{\theta JC}$	75	$^\circ C/W$
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	100	$^\circ C/W$

Notes: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins. $R_{\theta JA}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. $R_{\theta JA}$ shown below for single device operation on FR-4 PCB in still air.

ELECTRICAL SPECIFICATIONS ($T_A = 25^\circ\text{C}$ unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static ^(Note 3)						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = -250\mu A$	BV_{DSS}	-30	--	--	V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\mu A$	$V_{GS(TH)}$	-1.0	-1.5	-3.0	V
Gate Body Leakage	$V_{GS} = \pm 20V, V_{DS} = 0V$	I_{GSS}	--	--	± 100	nA
Zero Gate Voltage Drain Current	$V_{DS} = -24V, V_{GS} = 0V$	I_{DSS}	--	--	-1	μA
On-State Drain Current	$V_{DS} = -5V, V_{GS} = -10V$	$I_{D(ON)}$	-6	--	--	A
Drain-Source On-State Resistance	$V_{GS} = -10V, I_D = -3A$	$R_{DS(ON)}$	--	50	60	m Ω
	$V_{GS} = -4.5V, I_D = -2A$		--	75	90	
Forward Transconductance	$V_{DS} = -15V, I_D = -5A$	g_{fs}	4	7	--	S
Dynamic ^(Note 4)						
Total Gate Charge	$V_{DS} = -15V, I_D = -3A,$ $V_{GS} = -10V$	Q_g	--	9.52	--	nC
Gate-Source Charge		Q_{gs}	--	3.43	--	
Gate-Drain Charge		Q_{gd}	--	1.71	--	
Input Capacitance	$V_{DS} = -15V, V_{GS} = 0V,$ $f = 1.0\text{MHz}$	C_{iss}	--	551.57	--	pF
Output Capacitance		C_{oss}	--	90.96	--	
Reverse Transfer Capacitance		C_{rss}			60.79	
Switching ^(Note 5)						
Turn-On Delay Time	$V_{DD} = -15V,$ $R_{GEN} = 6\Omega,$ $I_D = -1A, V_{GS} = -10V,$	$t_{d(on)}$	--	10.8	--	ns
Turn-On Rise Time		t_r	--	2.33	--	
Turn-Off Delay Time		$t_{d(off)}$	--	22.53	--	
Turn-Off Fall Time		t_f	--	3.87	--	
Source-Drain Diode ^(Note 3)						
Forward On Voltage	$I_S = -1.9 A, V_{GS} = 0V$	V_{SD}	--	-0.8	-1.3	V

Notes:

1. Pulse width limited by the maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 5$ sec.
3. Pulse test: $PW \leq 300\mu s$, duty cycle $\leq 2\%$.
4. For DESIGN AID ONLY, not subject to production testing.
5. Switching time is essentially independent of operating temperature.

ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM3401CX RFG	SOT-23	3,000pcs / 7" Reel

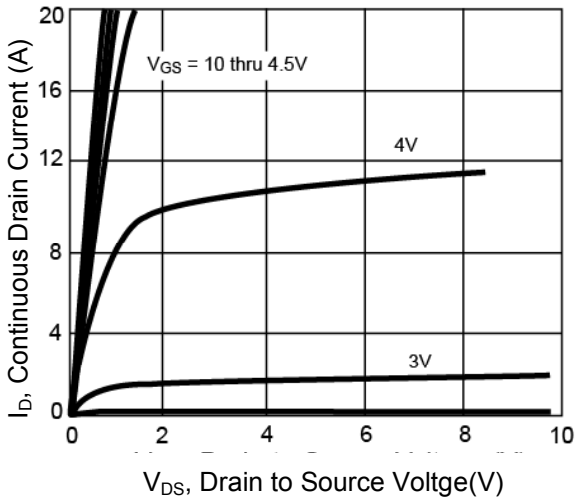
Note:

1. Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC
2. Halogen-free according to IEC 61249-2-21 definition

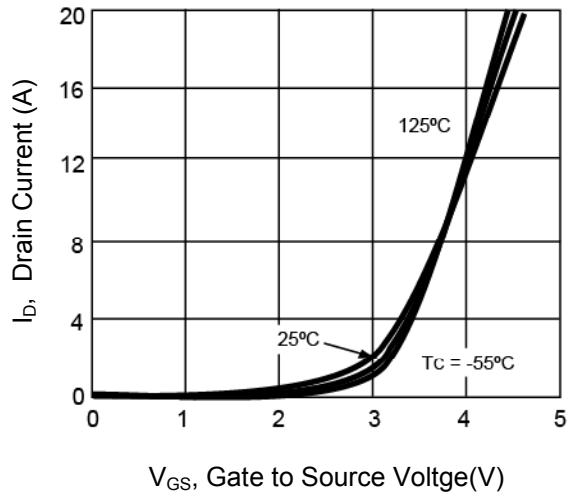
CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

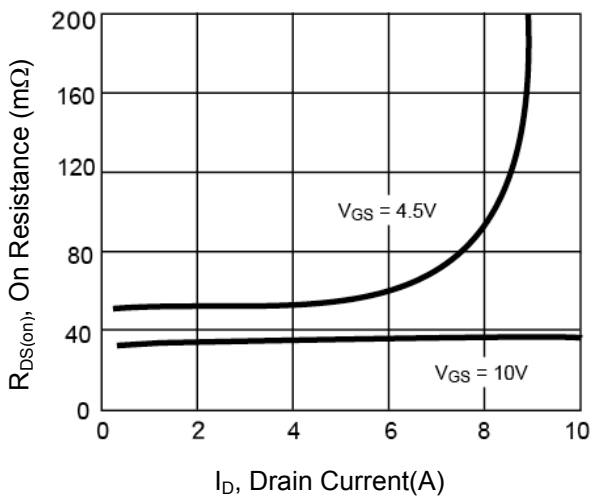
Output Characteristics



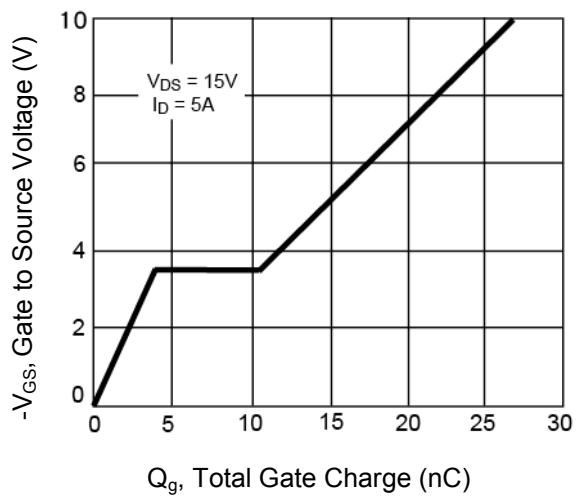
Transfer Characteristics



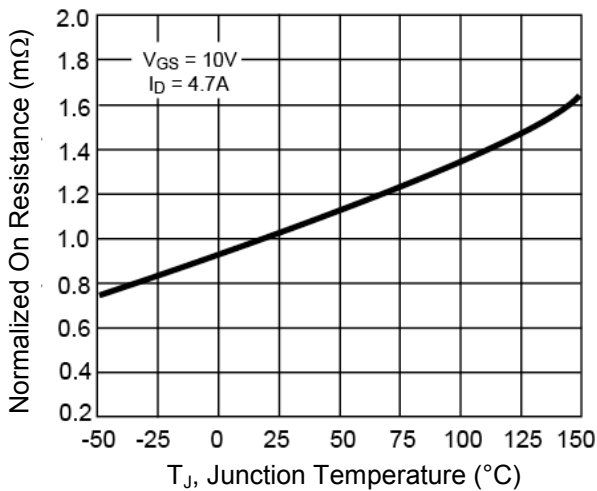
On-Resistance vs. Drain Current



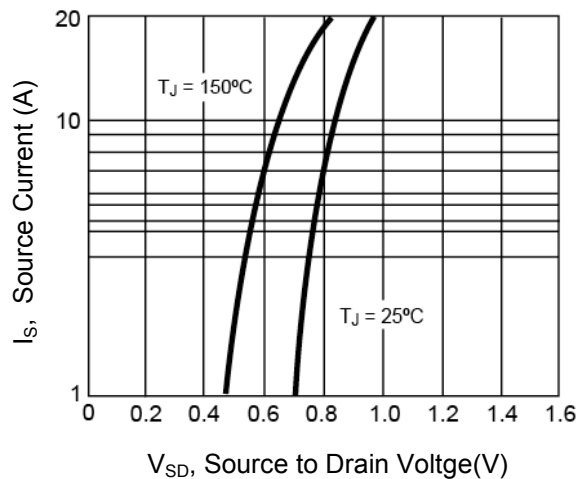
Gate Charge



On-Resistance vs. Junction Temperature



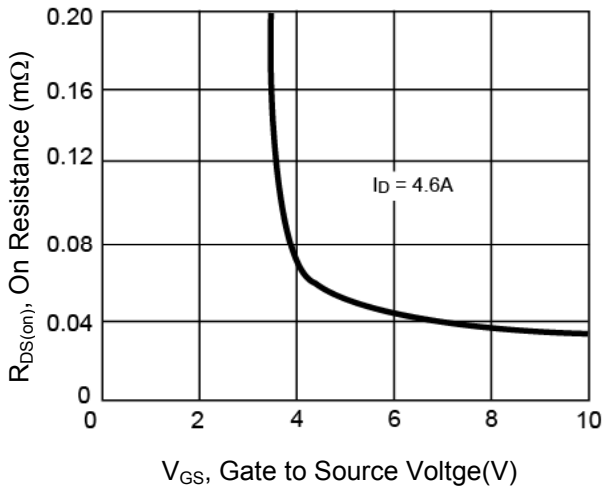
Source-Drain Diode Forward Voltage



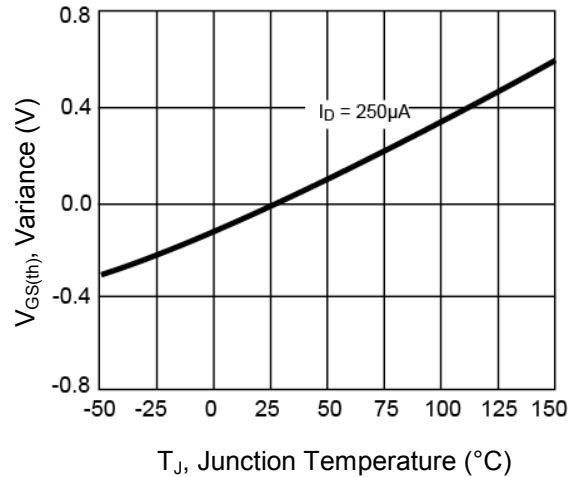
CHARACTERISTICS CURVES

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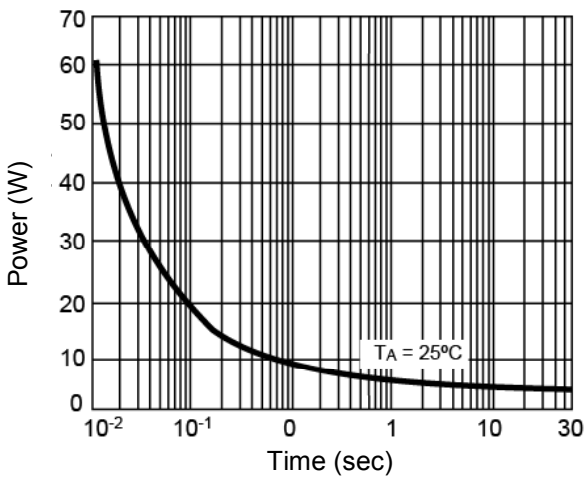
On-Resistance vs. Gate-Source Voltage



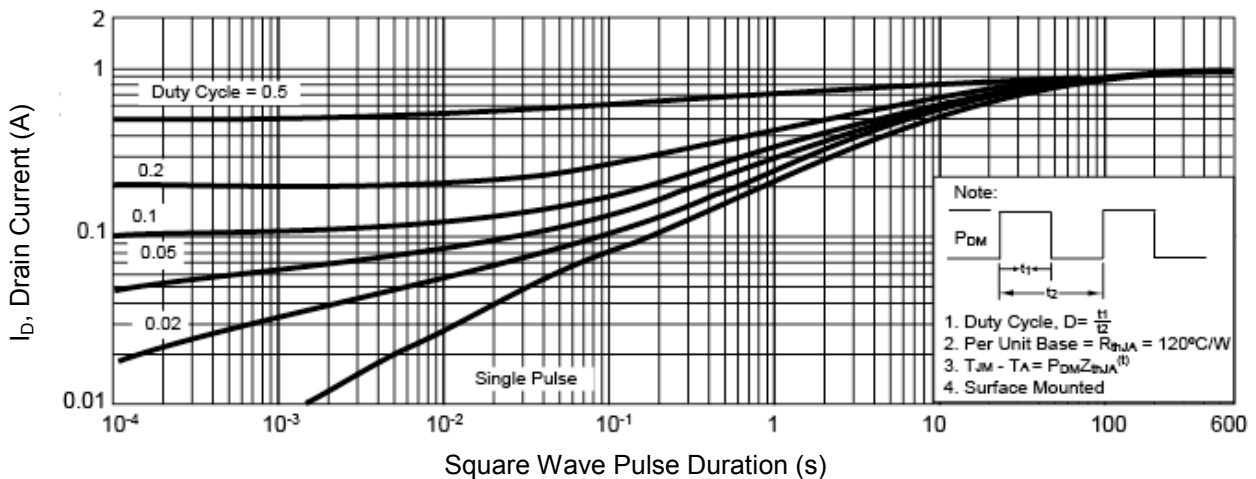
Threshold Voltage



Single Pulse Power

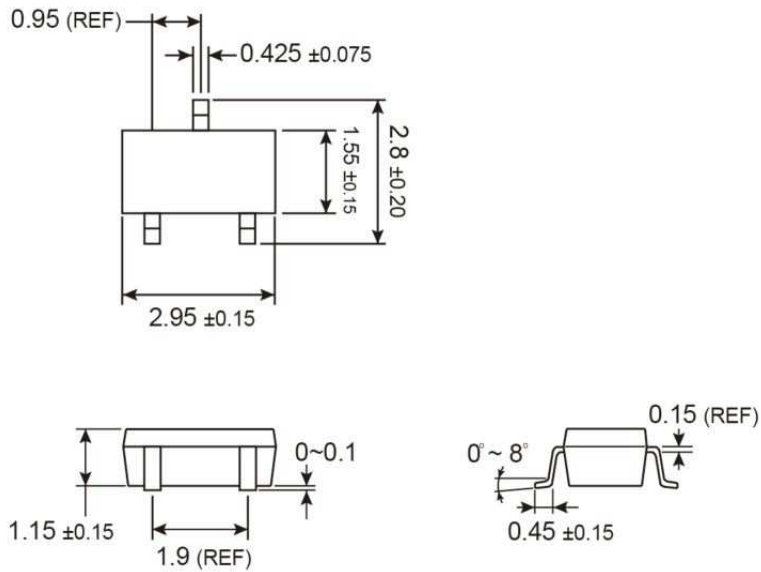


Normalized Thermal Transient Impedance Curve

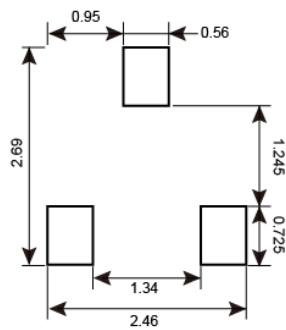


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

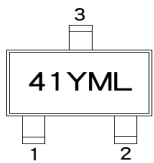
SOT-23



SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM



- Y** = Year Code
- M** = Month Code for Halogen Free Product
 - O** =Jan **P** =Feb **Q** =Mar **R** =Apr
 - S** =May **T** =Jun **U** =Jul **V** =Aug
 - W** =Sep **X** =Oct **Y** =Nov **Z** =Dec
- L** = Lot Code (1~9, A~Z)

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