

## SNx4LVC257A Quadruple 2-Line to 1-Line Data Selectors and Multiplexers With 3-State Outputs

### 1 Features

- Operate From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Maximum  $t_{pd}$  of 4.6 ns at 3.3 V
- Typical  $V_{OLP}$  (Output Ground Bounce)  $<0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  $>2$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
- On Products Compliant to MIL-PRF-38535, All Parameters Are Tested Unless Otherwise Noted. On All Other Products, Production Processing Does Not Necessarily Include Testing of All Parameters.

### 2 Applications

- Cable Modem Termination Systems
- Tests and Measurements
- I/O Expanders
- Motor Drivers
- Network Switches
- Servers
- Telecom Infrastructure

### 3 Description

These quadruple 2-line to 1-line data selectors and multiplexers are designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

The SNx4LVC257A devices are designed to multiplex signals from 4-bit data sources to 4-output data lines in bus-organized systems. The 3-state outputs do not load the data lines when the output-enable (OE) input is at a high logic level.

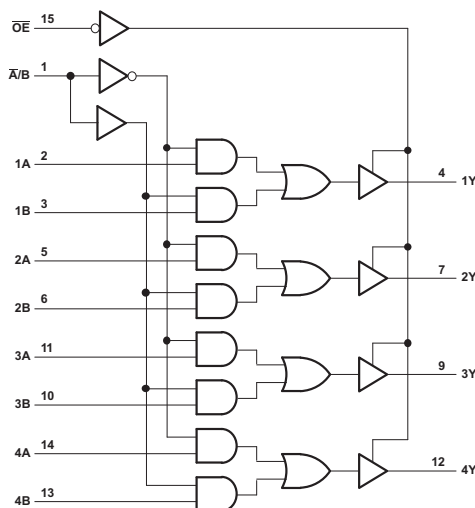
Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V or 5-V system environment.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LVC257A	VQFN (16)	3.50 mm × 4.00 mm
	SOIC (16)	9.90 mm × 3.91 mm
	SO (16)	10.30 mm × 5.30 mm
	SSOP (16)	5.50 mm × 6.20 mm
	TSSOP (16)	4.40 mm × 5.00 mm
SN54LVC257A	CDIP (16)	6.92 mm × 21.34 mm
	CFP (16)	10.30 mm × 6.73 mm
	LCCC (20)	8.89 mm × 8.89 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Logic Diagram (Positive Logic)



Pin numbers shown are for the D, DB, J, NS, PW, RGY, and W packages.



## Table of Contents

<b>1 Features</b> .....	<b>1</b>	9.1 Overview .....	<b>10</b>
<b>2 Applications</b> .....	<b>1</b>	9.2 Functional Block Diagram .....	<b>10</b>
<b>3 Description</b> .....	<b>1</b>	9.3 Feature Description .....	<b>10</b>
<b>4 Revision History</b> .....	<b>2</b>	9.4 Device Functional Modes .....	<b>10</b>
<b>5 Device Options</b> .....	<b>3</b>	<b>10 Application and Implementation</b> .....	<b>11</b>
<b>6 Pin Configuration and Functions</b> .....	<b>4</b>	10.1 Application Information .....	<b>11</b>
<b>7 Specifications</b> .....	<b>5</b>	10.2 Typical Application .....	<b>11</b>
7.1 Absolute Maximum Ratings .....	<b>5</b>	<b>11 Power Supply Recommendations</b> .....	<b>13</b>
7.2 ESD Ratings .....	<b>5</b>	<b>12 Layout</b> .....	<b>13</b>
7.3 Recommended Operating Conditions .....	<b>6</b>	12.1 Layout Guidelines .....	<b>13</b>
7.4 Thermal Information: 16-Pin Packages .....	<b>6</b>	12.2 Layout Example .....	<b>13</b>
7.5 Thermal Information: 20-Pin Package .....	<b>6</b>	<b>13 Device and Documentation Support</b> .....	<b>14</b>
7.6 Electrical Characteristics .....	<b>7</b>	13.1 Documentation Support .....	<b>14</b>
7.7 SN54LVC257A Switching Characteristics .....	<b>7</b>	13.2 Related Links .....	<b>14</b>
7.8 SN74LVC257A Switching Characteristics .....	<b>7</b>	13.3 Community Resources .....	<b>14</b>
7.9 Operating Characteristics .....	<b>8</b>	13.4 Trademarks .....	<b>14</b>
7.10 Typical Characteristics .....	<b>8</b>	13.5 Electrostatic Discharge Caution .....	<b>14</b>
<b>8 Parameter Measurement Information</b> .....	<b>9</b>	13.6 Glossary .....	<b>14</b>
<b>9 Detailed Description</b> .....	<b>10</b>	<b>14 Mechanical, Packaging, and Orderable Information</b> .....	<b>14</b>

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

### Changes from Revision N (June 2005) to Revision O

Page

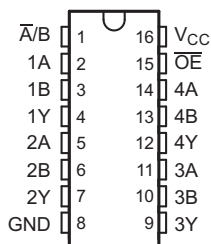
- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ..... **1**

## 5 Device Options

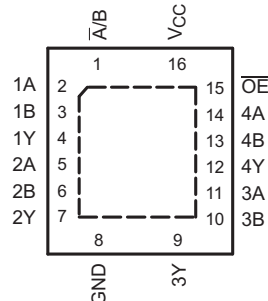
PART NUMBER	PACKAGE	BODY SIZE
SN74LVC257ARGYR	VQFN	3.50 mm × 4.00 mm
SN74LVC257AD	SOIC	3.90 mm × 9.90 mm
SN74LVC257ADT		
SN74LVC257ANSR	SO	5.30 mm × 10.10 mm
SN74LVC257ADBR	SSOP	5.50 mm × 6.20 mm
SN74LVC257APW	TSSOP	4.40 mm × 5.00 mm
SN74LVC257APWT		
SNJ54LVC257AJ	CDIP	6.92 mm × 21.34 mm
SNJ54LVC257AW	CFP	13.70 mm × 10.10 mm
SNJ54LVC257AFK	LCCC	8.89 mm × 8.89 mm

## 6 Pin Configuration and Functions

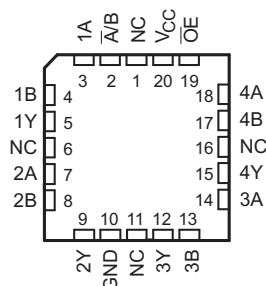
**D, DB, NS, J, W, or PW Package**  
**16-Pin SOIC, SSOP, SO, CDIP, CFP, or TSSOP**  
**Top View**



**RGY Package**  
**16-Pin VQFN with Exposed Thermal Pad**  
**Top View**



**FK Package**  
**20-Pin LCCC**  
**Top View**



### Pin Functions

NAME	PIN		I/O	DESCRIPTION
	SOIC, SSOP, SO, CDIP, CFP, TSSOP, or VQFN	LCCC		
$\bar{A}/B$	1	2	I	Select Pin, Low selects A, High selects B
1A	2	3	I/O	Multiplexer Signal Input
1B	3	4	I/O	Multiplexer Signal Input
1Y	4	5	I/O	Multiplexer Output
2A	5	7	I/O	Multiplexer Signal Input
2B	6	8	I/O	Multiplexer Signal Input
2Y	7	9	I/O	Multiplexer Output
3A	11	14	I/O	Multiplexer Signal Input
3B	10	13	I/O	Multiplexer Signal Input
3Y	9	12	I/O	Multiplexer Output
4A	14	18	I/O	Multiplexer Signal Input
4B	13	17	I/O	Multiplexer Signal Input
4Y	12	15	I/O	Multiplexer Output
GND	8	10	—	Ground
NC <sup>(1)</sup>	—	1, 6, 11, 16	—	No connect
$\bar{O}E$	15	19	I/O	Active low Output enable
V <sub>CC</sub>	16	20	—	Power pin

(1) NC – no internal connection

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT	
V <sub>CC</sub>	Supply voltage	-0.5	6.5	V	
V <sub>I</sub>	Input voltage <sup>(2)</sup>	-0.5	6.5	V	
V <sub>O</sub>	Output voltage <sup>(2) (3)</sup>	-0.5	V <sub>CC</sub> + 0.5	V	
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		-50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		-50	mA
I <sub>O</sub>	Continuous output current		±50	mA	
	Continuous current through V <sub>CC</sub> or GND		±100	mA	
T <sub>stg</sub>	Storage temperature	-65	150	°C	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V<sub>CC</sub> is provided in the recommended operating conditions table.

### 7.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

 See <sup>(1)</sup>

		SN54LVC257A		SN74LVC257A		UNIT
		MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	Operating		2	3.6	V
		Data retention only		1.5		
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V		0.65 × V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3 V to 2.7 V		1.7		
		V <sub>CC</sub> = 2.7 V to 3.6 V		2	2	
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V		0.35 × V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3 V to 2.7 V		0.7		
		V <sub>CC</sub> = 2.7 V to 3.6 V		0.8		
V <sub>I</sub>	Input voltage	0	5.5	0	5.5	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 1.65 V		–4		mA
		V <sub>CC</sub> = 2.3 V		–8		
		V <sub>CC</sub> = 2.7 V		–12		
		V <sub>CC</sub> = 3 V		–24		
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.65 V		4		mA
		V <sub>CC</sub> = 2.3 V		8		
		V <sub>CC</sub> = 2.7 V		12		
		V <sub>CC</sub> = 3 V		24		
Δt/Δv	Input transition rise or fall rate	10		10		ns/V
T <sub>A</sub>	Operating free-air temperature	–55	125	–40	85	°C

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

### 7.4 Thermal Information: 16-Pin Packages

THERMAL METRIC <sup>(1)</sup>	SN54LVC257A, SN74LVC257A				UNIT	
	D (SOIC) <sup>(2)</sup>	DB (SSOP) <sup>(2)</sup>	NS (SO) <sup>(2)</sup>	PW (TSSOP) <sup>(2)</sup>		
	16 PINS					
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	73	82	64	108	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

(2) The package thermal impedance is calculated in accordance with JESD 51-7.

### 7.5 Thermal Information: 20-Pin Package

THERMAL METRIC <sup>(1)</sup>	SN54LVC257A		UNIT
	RGY (LCCC) <sup>(2)</sup>		
	20 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	39	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

(2) The package thermal impedance is calculated in accordance with JESD 51-5.

## 7.6 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	SN54LVC257A			SN74LVC257A			UNIT
			MIN	TYP <sup>(1)</sup>	MAX	MIN	TYP <sup>(1)</sup>	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -100 μA	1.65 V to 3.6 V				V <sub>CC</sub> - 0.2			V
	I <sub>OH</sub> = -100 μA	2.7 V to 3.6 V	V <sub>CC</sub> - 0.2						
	I <sub>OH</sub> = -4 mA	1.65 V				1.2			
	I <sub>OH</sub> = -8 mA	2.3 V				1.7			
	I <sub>OH</sub> = -12 mA	2.7 V	2.2			2.2			
		3 V	2.4			2.4			
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA	1.65 V to 3.6 V				0.2			V
		2.7 V to 3.6 V	0.2						
	I <sub>OL</sub> = 4 mA	1.65 V				0.45			
	I <sub>OL</sub> = 8 mA	2.3 V				0.7			
	I <sub>OL</sub> = 12 mA	2.7 V	0.4			0.4			
3 V		0.55			0.55				
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	3.6 V				±5			μA
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	3.6 V				±15			μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6 V	10			10			μA
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	2.7 V to 3.6 V	500			500			μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V	5			5			pF
C <sub>o</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V	5			5			pF

(1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

## 7.7 SN54LVC257A Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVC257A				UNIT
			V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A or B	Y	5.4		1 4.6		ns
	$\overline{A/B}$		7.5		1 6.4		
t <sub>en</sub>	$\overline{OE}$	Y	6.7		1 5.6		ns
t <sub>dis</sub>	$\overline{OE}$	Y	4.7		0.5 4.3		ns
t <sub>sk(o)</sub>					1		ns

## 7.8 SN74LVC257A Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC257A								UNIT
			V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A or B	Y	1	13.5	1	7.4	1	5.4	1	4.6	ns
	$\overline{A/B}$		1	15.6	1	9.5	1	7.5	1	6.4	
t <sub>en</sub>	$\overline{OE}$	Y	1	14.6	1	8.7	1	6.7	1	5.6	ns
t <sub>dis</sub>	$\overline{OE}$	Y	1	15.4	1	6.7	1	4.7	1	4.3	ns
t <sub>sk(o)</sub>									1		ns

# SN54LVC257A, SN74LVC257A

SCAS2940 – JANUARY 1993 – REVISED JUNE 2015

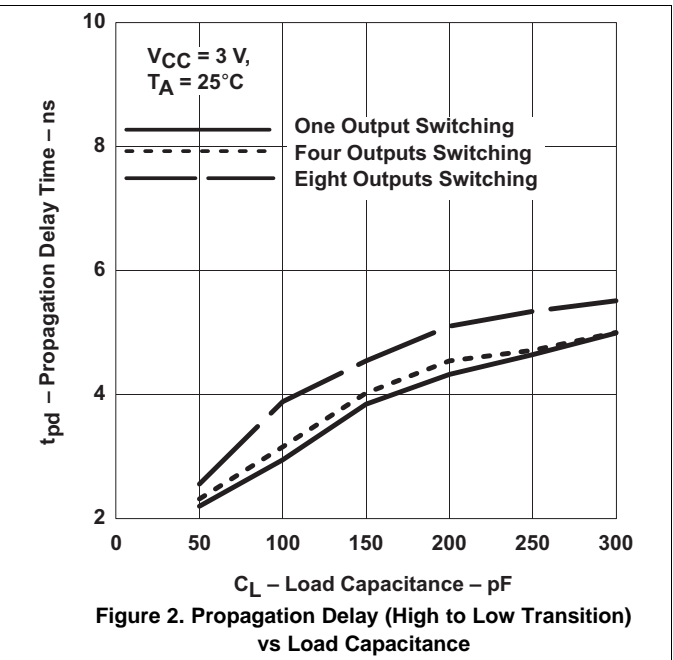
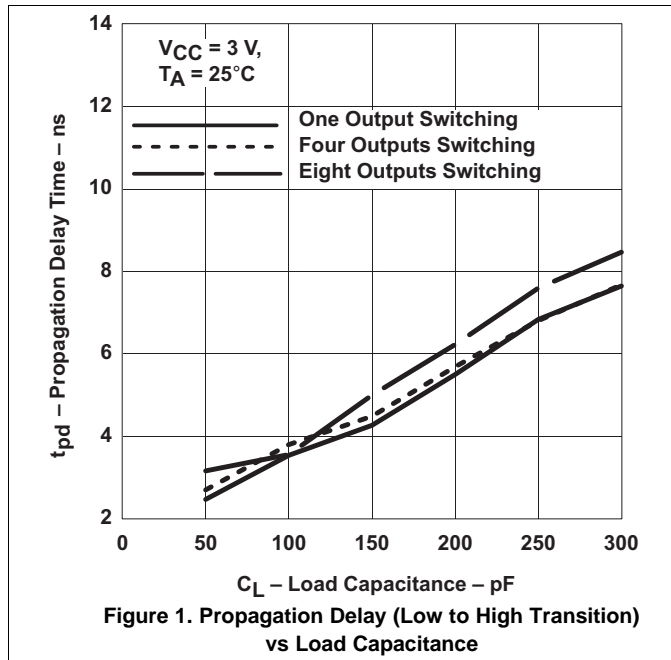
www.ti.com

## 7.9 Operating Characteristics

$T_A = 25^\circ\text{C}$

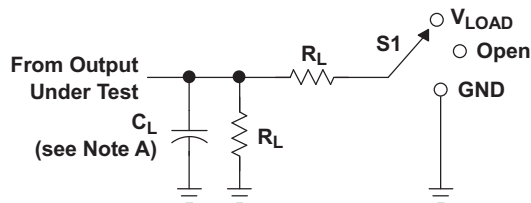
PARAMETER	TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V}$	$V_{CC} = 3.3\text{ V}$	UNIT
		TYP	TYP	TYP	
$C_{pd}$ Power dissipation capacitance	$f = 10\text{ MHz}$	13.5	14.5	15.5	pF

## 7.10 Typical Characteristics





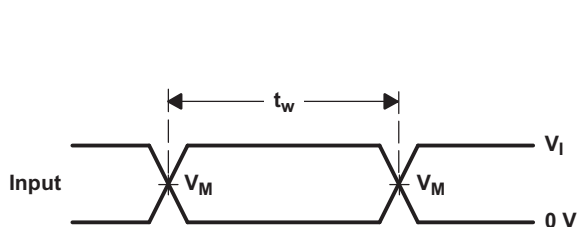
## 8 Parameter Measurement Information



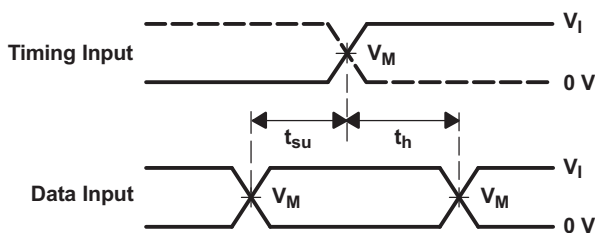
LOAD CIRCUIT

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

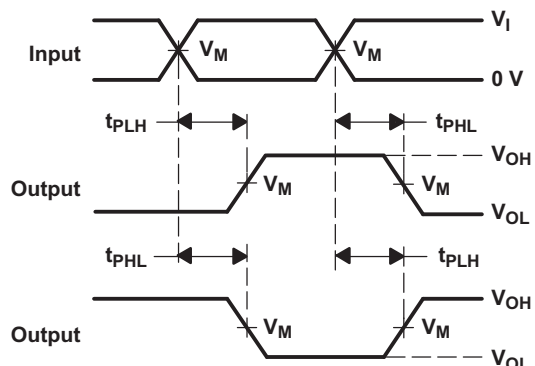
$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_r/t_f$					
1.8 V±0.15 V	$V_{CC}$	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 kΩ	0.15 V
2.5 V±0.2 V	$V_{CC}$	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500Ω	0.15 V
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500Ω	0.3 V
3.3 V±0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500Ω	0.3 V



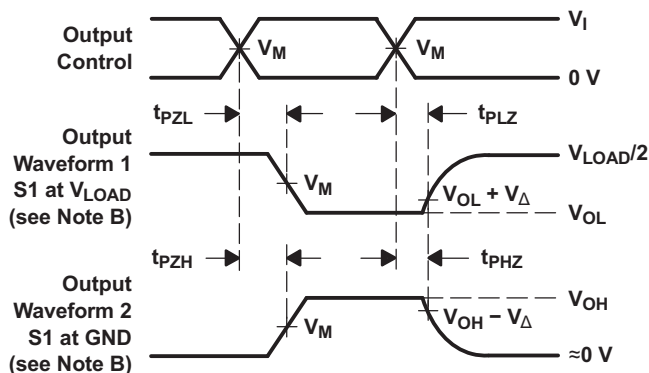
VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR ≤10 MHz,  $Z_O = 50 \Omega$ .
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

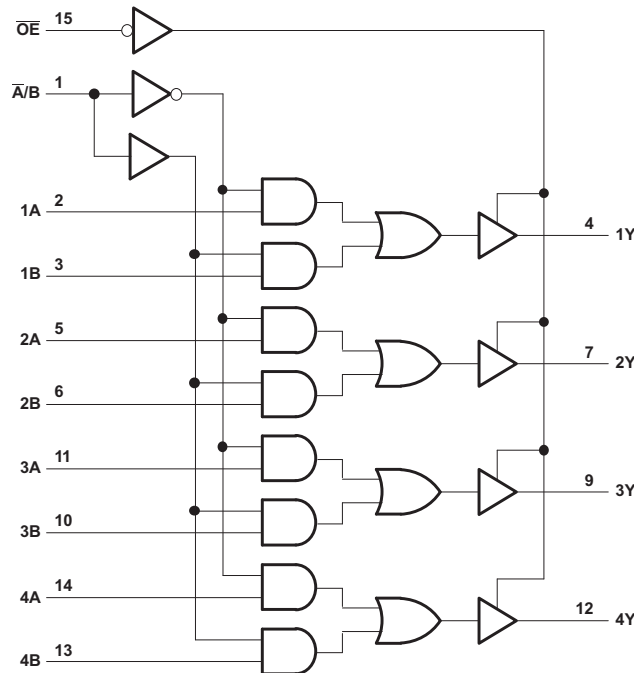
## 9 Detailed Description

### 9.1 Overview

These quadruple 2-line to 1-line data selectors and multiplexers are designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

The SNx4LVC257A devices are designed to multiplex signals from 4-bit data sources to 4-output data lines in bus-organized systems. The 3-state outputs do not load the data lines when the output-enable ( $\overline{OE}$ ) input is at a high logic level.

### 9.2 Functional Block Diagram



### 9.3 Feature Description

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V and 5-V system environment. Device features a maximum  $t_{pd}$  of 4.6 ns allowing the device to be used in high-speed applications as well.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  must be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

### 9.4 Device Functional Modes

Table 1 lists the functional modes for the SN54LVC257A and SN74LVC257A devices.

Table 1. Function Table

INPUTS				OUTPUT Y
$\overline{OE}$	$\overline{A/B}$	A	B	
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

## 10 Application and Implementation

### NOTE

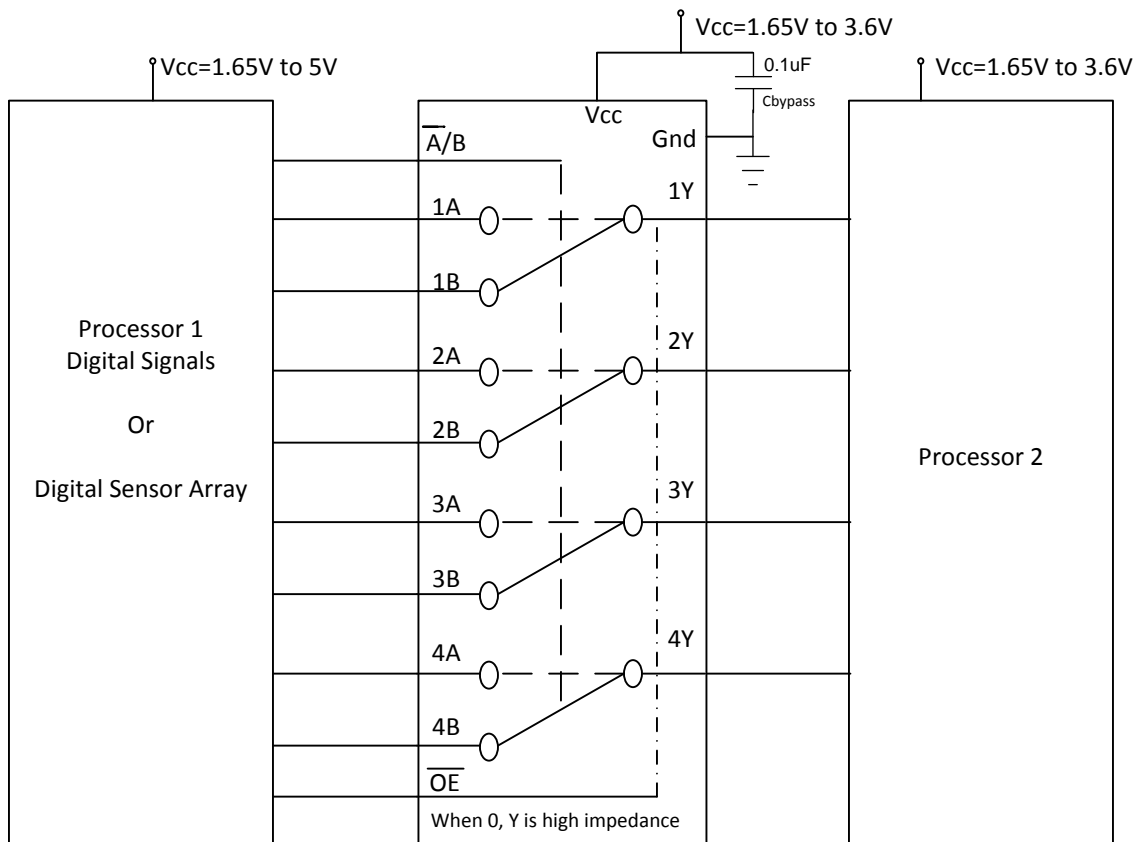
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 10.1 Application Information

The SNx4LVC257A devices are useful for digital signal data selector or multiplexer applications.

### 10.2 Typical Application

The SNx4LVC257A devices use CMOS technology and have balanced output drive. These devices can be used for down level translation and multiplexer function as shown in [Figure 4](#).



**Figure 4. SNx4LVC257A Used as Level Translation and as a Multiplexer**

#### 10.2.1 Design Requirements

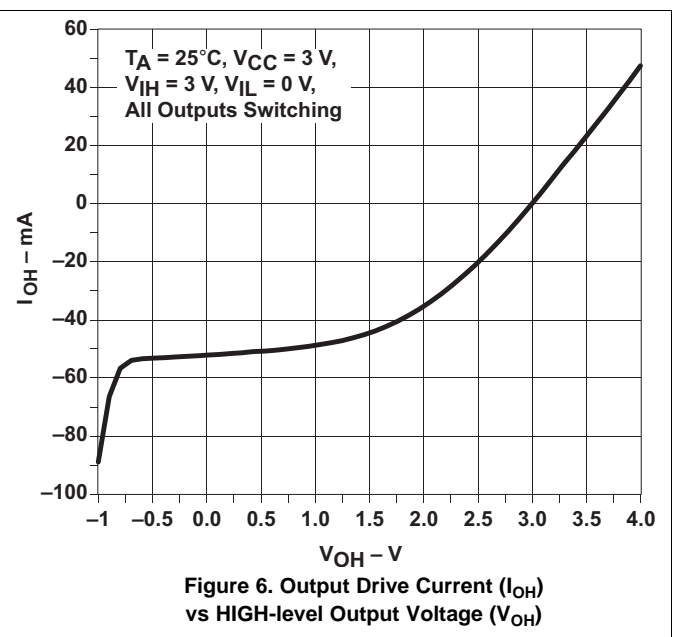
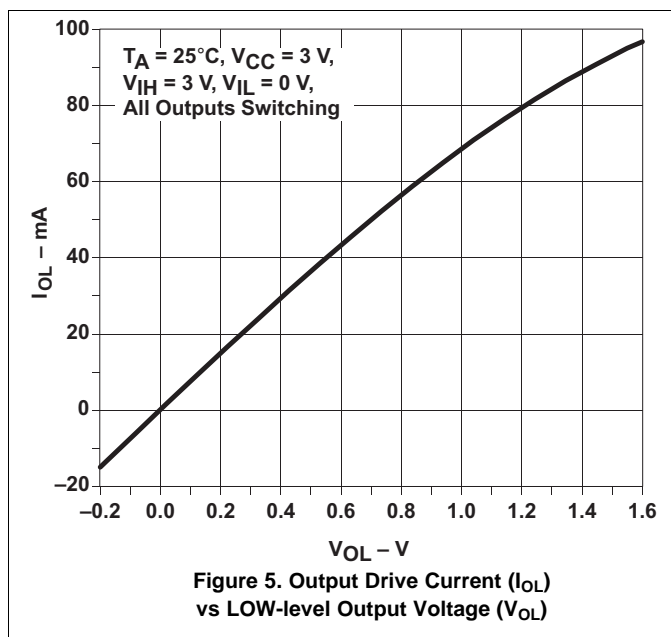
Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions must be considered to prevent ringing.

## Typical Application (continued)

### 10.2.2 Detailed Design Procedure

1. Recommended Input Conditions
  - For rise time and fall time specification, see  $(\Delta t/\Delta V)$  in the [Recommended Operating Conditions](#) table.
  - For specified high and low levels, see  $(V_{IH}$  and  $V_{IL})$  in the [Recommended Operating Conditions](#) table.
  - Inputs are over voltage tolerant allowing them to go as high as  $(V_I \text{ max})$  in the [Recommended Operating Conditions](#) table at any valid  $V_{CC}$ .
2. Recommend Output Conditions
  - Load currents must not exceed  $(I_O \text{ max})$  per output and must not exceed (continuous current through  $V_{CC}$  or GND) total current for the part. These limits are in the [Recommended Operating Conditions](#) table.
  - Outputs must not be pulled above  $V_{CC}$ .

### 10.2.3 Application Curves



## 11 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each  $V_{CC}$  terminal must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- $\mu\text{F}$  capacitor is recommended. If there are multiple  $V_{CC}$  terminals then 0.01- $\mu\text{F}$  or 0.022- $\mu\text{F}$  capacitors are recommended for each power terminal. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. Multiple bypass capacitors may be paralleled to reject different frequencies of noise. The bypass capacitor must be installed as close to the power terminal as possible for the best results.

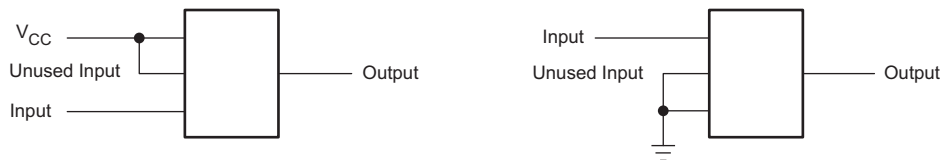
## 12 Layout

### 12.1 Layout Guidelines

When using multiple bit logic devices, inputs must not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in [Figure 7](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient.

### 12.2 Layout Example



**Figure 7. Layout Diagrams**

## 13 Device and Documentation Support

### 13.1 Documentation Support

#### 13.1.1 Related Documentation

For related documentation see the following:

*Implications of Slow or Floating CMOS Inputs*, [SCBA004](#)

### 13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 2. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54LVC257A	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
SN74LVC257A	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 13.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 13.4 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

### 13.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 13.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-0050901QFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-0050901QF A SNJ54LVC257AW	<a href="#">Samples</a>
SN74LVC257AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC257A	<a href="#">Samples</a>
SN74LVC257ADBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC257A	<a href="#">Samples</a>
SN74LVC257ADBRE4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC257A	<a href="#">Samples</a>
SN74LVC257ADBRG4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC257A	<a href="#">Samples</a>
SN74LVC257ADG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC257A	<a href="#">Samples</a>
SN74LVC257ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC257A	<a href="#">Samples</a>
SN74LVC257ADRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC257A	<a href="#">Samples</a>
SN74LVC257ADT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC257A	<a href="#">Samples</a>
SN74LVC257ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC257A	<a href="#">Samples</a>
SN74LVC257APW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC257A	<a href="#">Samples</a>
SN74LVC257APWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC257A	<a href="#">Samples</a>
SN74LVC257APWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC257A	<a href="#">Samples</a>
SN74LVC257APWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-40 to 85	LC257A	<a href="#">Samples</a>
SN74LVC257APWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC257A	<a href="#">Samples</a>
SN74LVC257APWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC257A	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC257APWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC257A	<a href="#">Samples</a>
SN74LVC257ARGYR	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LC257A	<a href="#">Samples</a>
SNJ54LVC257AW	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-0050901QF A SNJ54LVC257AW	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and



continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54LVC257A, SN74LVC257A :**

- Catalog: [SN74LVC257A](#)
- Automotive: [SN74LVC257A-Q1](#), [SN74LVC257A-Q1](#)
- Enhanced Product: [SN74LVC257A-EP](#), [SN74LVC257A-EP](#)
- Military: [SN54LVC257A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC257ADBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74LVC257ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LVC257ANSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LVC257APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC257APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC257APWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC257APWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC257ARGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC257ADBR	SSOP	DB	16	2000	367.0	367.0	38.0
SN74LVC257ADR	SOIC	D	16	2500	333.2	345.9	28.6
SN74LVC257ANSR	SO	NS	16	2000	367.0	367.0	38.0
SN74LVC257APWR	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74LVC257APWR	TSSOP	PW	16	2000	364.0	364.0	27.0
SN74LVC257APWRG4	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74LVC257APWT	TSSOP	PW	16	250	367.0	367.0	35.0
SN74LVC257ARGYR	VQFN	RGY	16	3000	367.0	367.0	35.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP2-F16

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



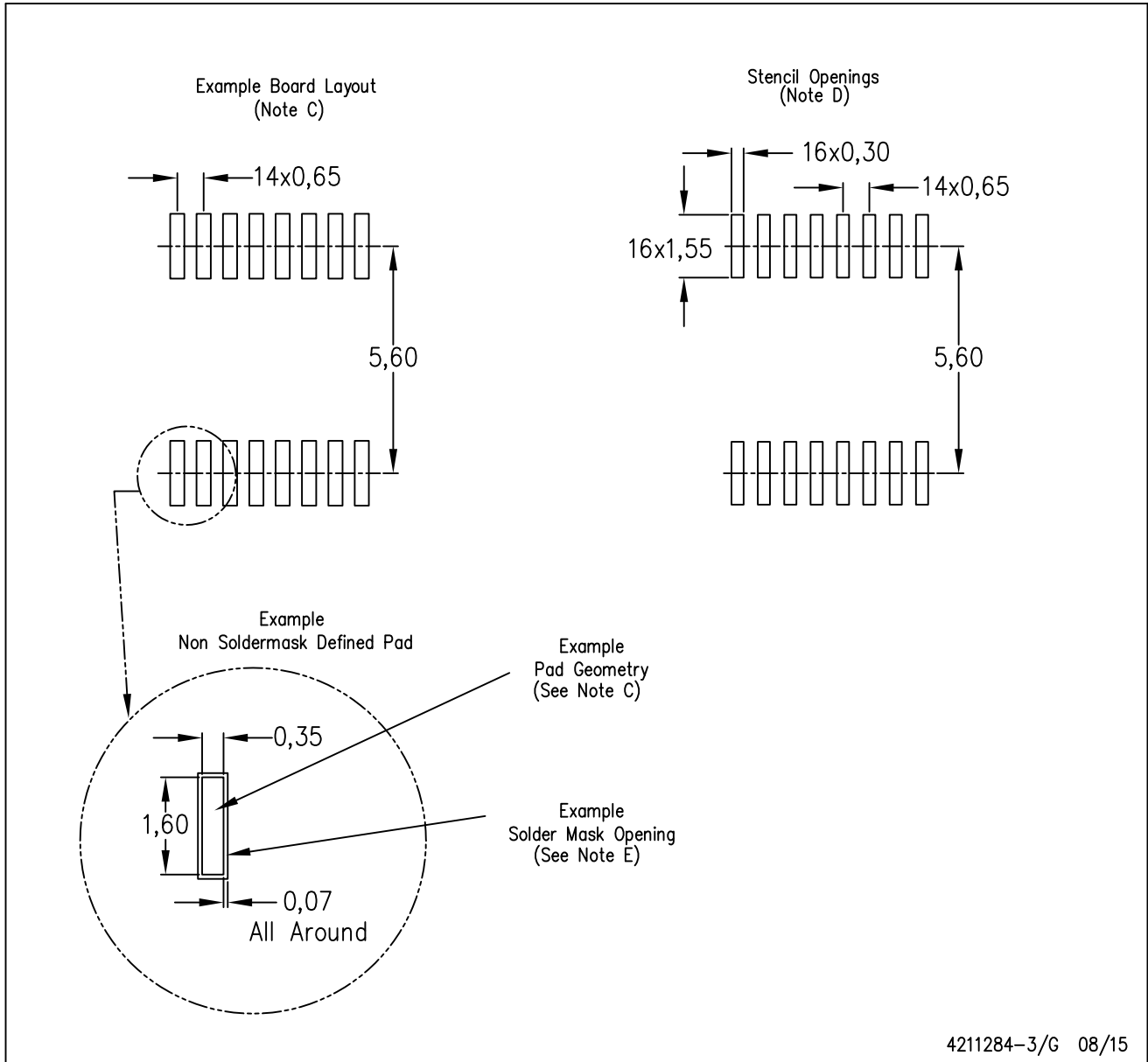
4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153



PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

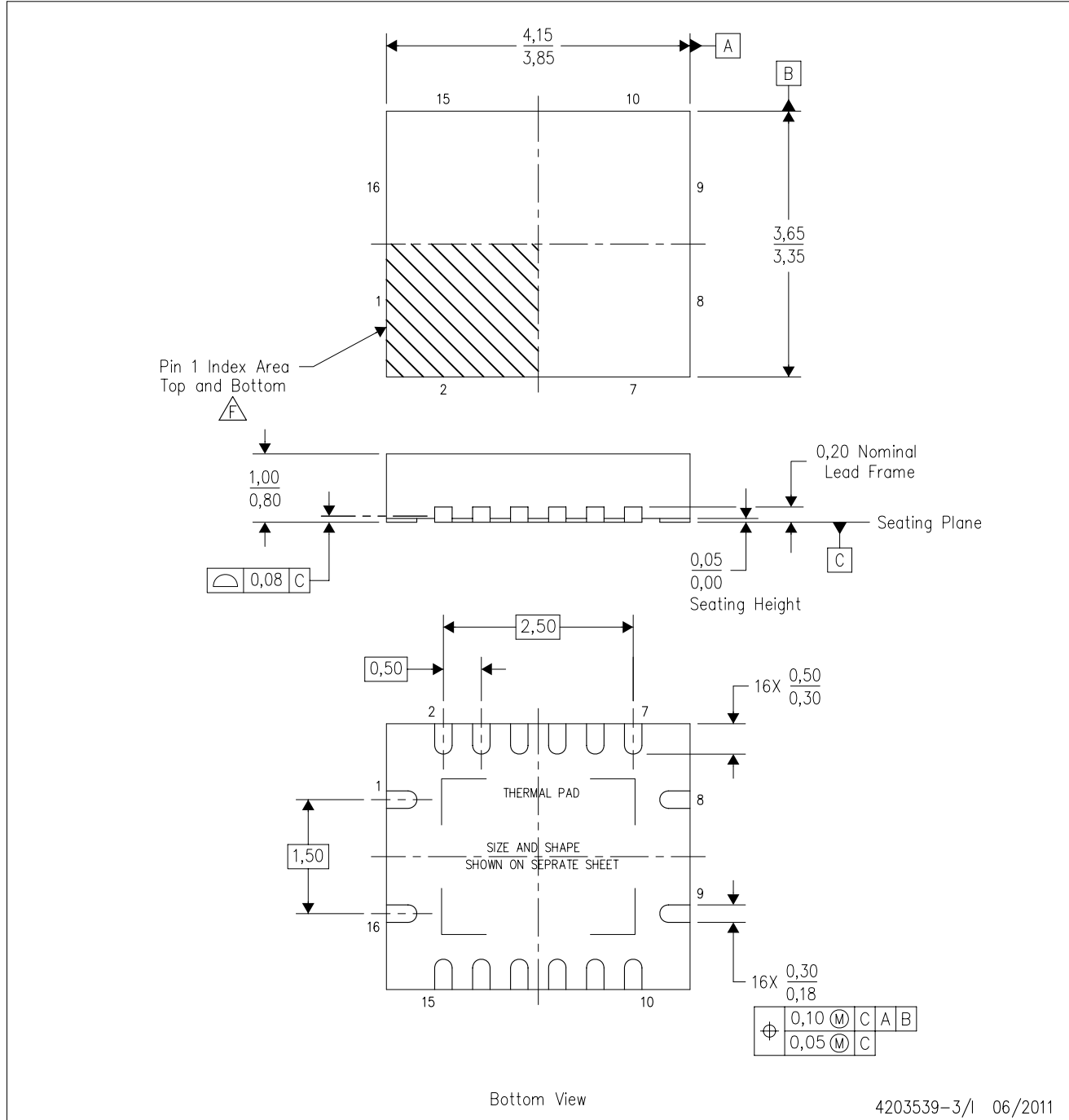
28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) package configuration.
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - G. Package complies to JEDEC MO-241 variation BA.

RGY (R-PVQFN-N16)

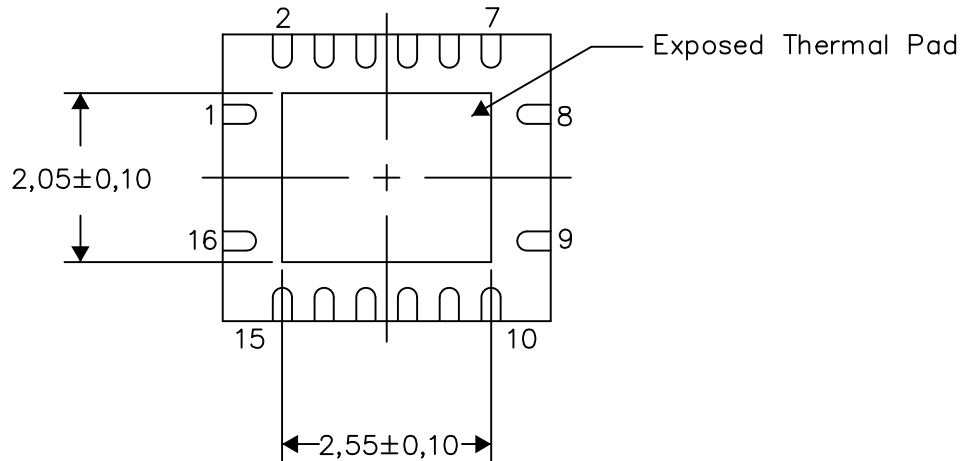
PLASTIC QUAD FLATPACK NO-LEAD

**THERMAL INFORMATION**

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

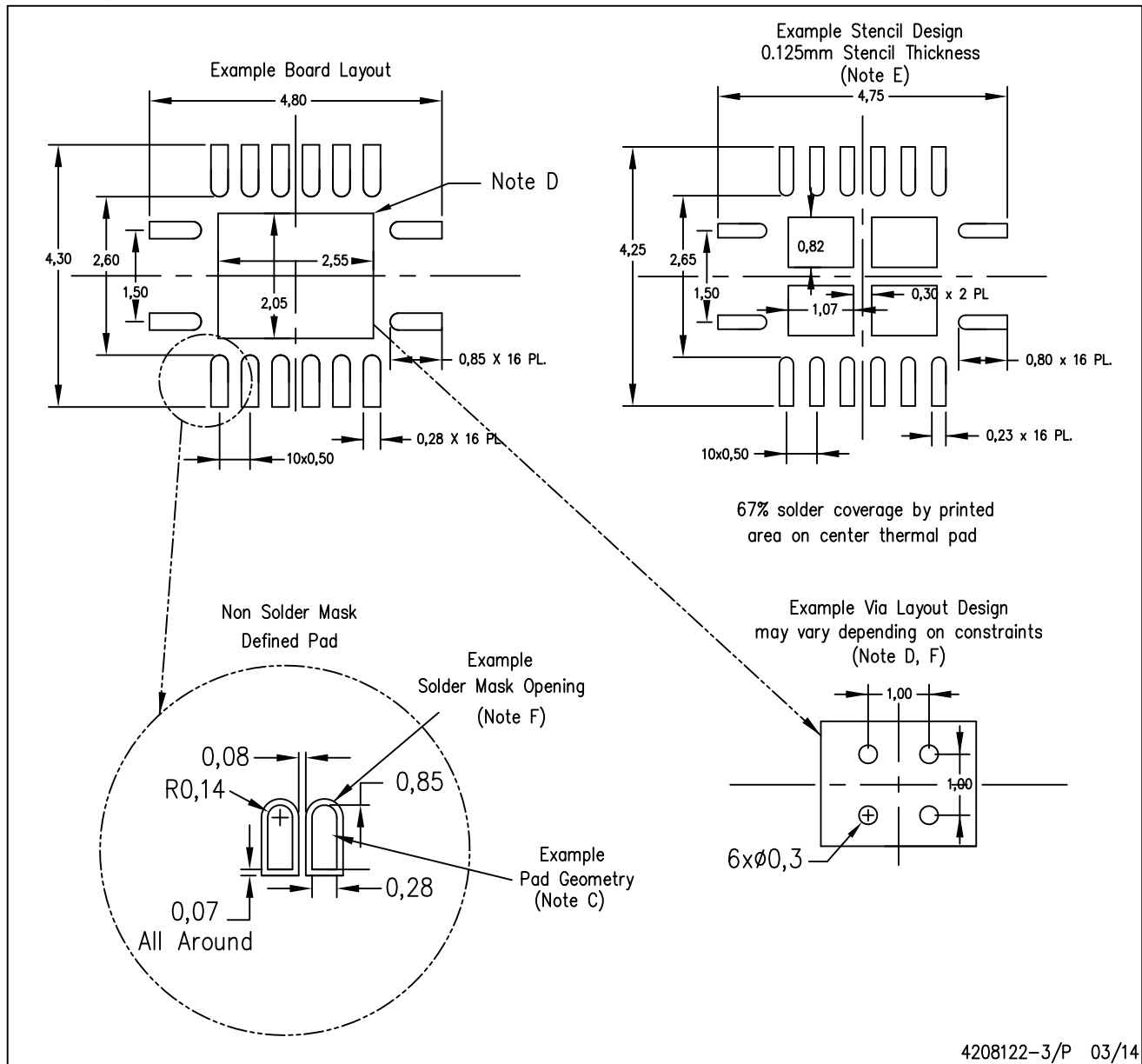
Exposed Thermal Pad Dimensions

4206353-3/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

## IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.