#### SDLS027

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

#### description

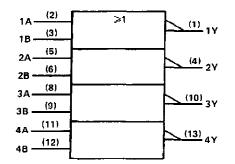
These devices contain four independent 2-input-NOR gates.

The SN5402, SN54LS02, and SN54S02 are characterized for operation over the full military temperature range of -55 °C to 125 °C. The SN7402, SN74LS02, and SN74S02 are characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE	(each	gate)	
----------------	-------	-------	--

INP	UTS	OUTPUT
A	в	Y
н	x	L
х	н	L
L	L	н

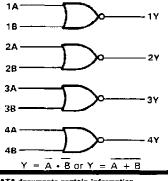
logic symbol<sup>†</sup>



<sup>†</sup>This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

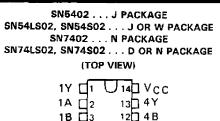
#### logic diagram (positive logic)



PRODUCTION DATA documents contain information current as of publication dats. Preducts conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include tasting of all parameters.

## SN5402, SN54LS02, SN54S02, SN7402, SN74LS02, SN74S02 QUADRUPLE 2-INPUT POSITIVE-NOR GATES

DECEMBER 1983-REVISED MARCH 1988

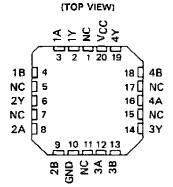


2Y 🗖	4	11 4A
2A 🗌	5	10 J 3 Y
2B 🖸	6	9 <mark>5</mark> 3 ₿
	7	8 🛛 3 A

SN5402 ... W PACKAGE (TOP VIEW)

1A 🗆	1	U	14	Ь	4Y
18 🗌	2		13	þ	4B
1Y 🗆	3		12	þ	4A
Vcc □	4	•	11	þ	GND
2Y 🗋	5		10	þ	3B
2A 🗌	6		9	þ	3A
2B 🗖	7		8	Þ	3Y

SN54LS02, SN54S02 ... FK PACKAGE

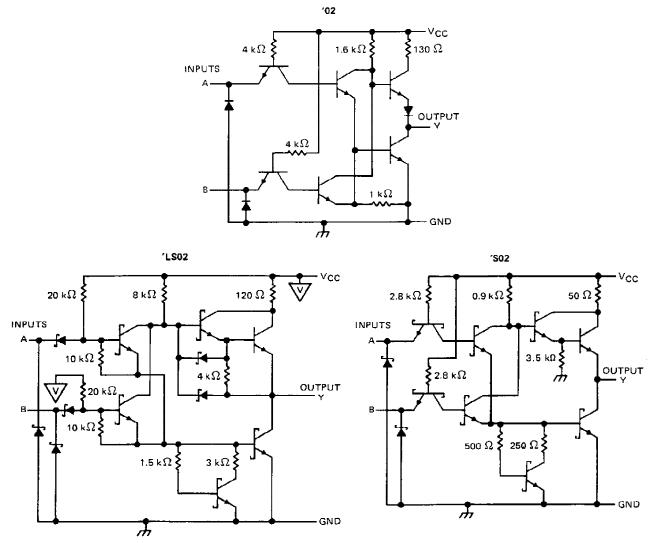


NC - No internal connection



## SN5402, SN54LS02, SN54S02, SN7402, SN74LS02, SN74S02 QUADRUPLE 2-INPUT POSITIVE-NOR GATES

schematics (each gate)



Resistor values shown are nominal.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1)	<b>7</b> V
Input voltage: '02, 'SO2	
'LS02	<b>7 V</b>
Off-state output voltage	7V
Operating free-air temperature range: SN54'	55°C to 125°C
SN74'	
Storage temperature range	65°C to 150°C

NOTE 1. Voltage values are with respect to network ground terminal.



## SN5402, SN7402 QUADRUPLE 2-INPUT POSITIVE-NOR GATES

#### recommended operating conditions

	:	SN5402			SN7402			
	MIN	NOM	MAX	MIN	NOM	мах	UNIT	
V <sub>CC</sub> Supply voltage	4.5	5	5.5	4.75	5	5.25	ν	
VIH High-level input voltage	2			2			v	
VIL Low-level input voltage			0.8			0.8	v	
IOH High-level output current			- 0.4			- 0.4	mΑ	
IOL Low-level output current			16			16	mΑ	
TA Operating free-air temperature	55		125	0		70	°c	

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

		TEST CONDITIONS T			SN5402			SN7402			
PARAMETER				MIN	TYP‡	MAX	MIN	түр‡	MAX	UNIT	
¥ικ	V <sub>CC</sub> = MIN,	l₁ = − 12 mA				- 1.5			- 1.5	V	
∨он	V <sub>CC</sub> = MIN,	V <sub>IL</sub> = 0.8 V,	I <sub>OH</sub> = - 0.4 mA	2.4	3.4		2.4	3.4		V	
V <sub>OL</sub>	V <sub>CC</sub> = MIN,	V <sub>IH</sub> = 2 V,	I <sub>OL</sub> = 16 mA		0.2	0.4		0.2	0.4	V	
4	V <sub>CC</sub> = MAX,	V <sub>1</sub> = 5.5 V				1			1	mA	
<sup>I</sup> IH	V <sub>CC</sub> = MAX,	Vi = 2.4 V	- -			40			40	μA	
hι	V <sub>CC</sub> = MAX,	V <sub>1</sub> = 0.4 V				- 1. <b>6</b>			— 1. <b>6</b>	mА	
los∮	VCC = MAX			- 20		- 55	- 18		- 55	mA	
<sup>I</sup> ССН	V <sub>CC</sub> = MAX,	V <sub>1</sub> = 0 V			8	16		8	16	mΑ	
ICCL	V <sub>CC</sub> = MAX,	See Note 2			14	27		14	27	mA	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 V$ ,  $T_A = 25^{\circ}C$ .

\$ Not more than one output should be shorted at a time.

NOTE 2: One input at 4.5 V, ell others at GND.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C (see note 3)

PARAMETER	FROM (INPUT)	то (о <b>υт</b> рит)	TEST CONDITIONS	MIN	түр	МАХ	UNIT
tPLH		N			12	22	ns
<sup>t</sup> PHL	A or B	Ŷ	R <sub>L</sub> = 400 Ω, C <sub>L</sub> = 15 pF		8	15	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



## SN54LS02, SN74LS02 QUADRUPLE 2-INPUT POSITIVE NOR GATES

#### recommended operating conditions

			SN54LS02			SN74LS02			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Vcc	Supply voltage	4.5	5	5.5	4.75	5	5.25	v	
VIH	High-level input voltage	2			2			v	
۷i۲	Low-level input voltage			0.7			0.8	V	
юн	High-level output current			- 0.4			- 0.4	mΑ	
10L	Low-level output current			4			8	mΑ	
Тд	Operating free-air temporature	- 55		125	0		70	°c	

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

		TEST CONDITIONS T			SN54LS02			SN74LS02		
PARAMETER	153			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
۷ıĸ	V <sub>CC</sub> = MIN, I <sub>1</sub> =	- 18 mA				- 1.5			- 1.5	V
√он	V <sub>CC</sub> = MIN, V <sub>IL</sub>	= MAX,	<sup>†</sup> OH = - 0.4 mA	2.5	3.4		2.7	3.4		v
	V <sub>CC</sub> = MIN, V <sub>I</sub>	⊣=2V,	l <sub>OL</sub> = 4 mA		0.25	0.4		0.25	0.4 V	
VOL	V <sub>CC</sub> = MIN, V <sub>IF</sub>	⊣=2V,	IOL = 8 mA					0.35	0.5	ľ
4	V <sub>CC</sub> = MAX, V <sub>I</sub> -	= 7 V				0.1			0.1	mΑ
ίн	VCC = MAX, VI	= 2.7 V	······································			20			20	μA
μL	VCC = MAX, VI	= 0.4 V				- 0.4			- 0.4	mΑ
los§	V <sub>CC</sub> - MAX		· ····	- 20		- 100	- 20		- 100	mΑ
Іссн	V <sub>CC</sub> = MAX, VI	= 0 V	•		1.6	3.2		1.6	3.2	mΑ
ICCL	VCC = MAX, See	Note 2			2.8	5.4		2.8	5.4	mА

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

 $\pm$  All typical values are at V<sub>C</sub> = 5 V, T<sub>A</sub> = 25<sup>o</sup>C § Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second. NOTE 2: One input at 4.5 V, all others at GND.

## switching characteristics, VCC = 5 V, TA = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CON	DITIONS	MIN	түр	МАХ	UNIT
₹₽LH	A or B	Ŷ	P 340	C. = 15 pE		10	15	ńs
<sup>t</sup> PHL	2010	•	RL = 2 kΩ,	C <sub>L</sub> = 15 pF		10	15	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

# SN54S02, SN74S02 QUADRUPLE 2-INPUT POSITIVE-NOR GATES

#### recommended operating conditions

			SN54S02			SN74S02		
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
V <sub>CC</sub> Supply volta	8ge	4.5	5	5.5	4.75	5	5.25	v
V <sub>IH</sub> High-level in	nput voltage	2			2			v
VIL Low-level in	iput voltage			0.8			0.8	v
IOH High-level o	utput current			- 1			- 1	mΑ
IOL Low-level of	utput current			20			20	mA
T <sub>A</sub> Operating fr	ree-air temperature	55		125	0		70	°c

\*

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS T	SN54S02	SN74802	UNIT
		MIN TYP‡ MAX	MIN TYP‡ MAX	
۷ <sub>IK</sub>	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA	-1.2	-1.2	v
V <sub>OH</sub>	$V_{CC} = MIN$ , $V_{L} = 0.8 V$ , $i_{OH} = -1 mA$	2.5 3.4	2.7 3.4	v
VOL	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, I <sub>OL</sub> = 20 mA	0.5	0.5	V
4	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V	1	1	mA
—————————————————————————————————————	V <sub>CC</sub> = MAX, V <sub>1</sub> = 2.7 V	50	50	μA
ΙL	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5 V	-2	-2	mA
I <sub>OS</sub> §	V <sub>CC</sub> = MAX	-40 -100	-40 -100	mA
ссн	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0 V	17 29	17 29	mA
ICCL	V <sub>CC</sub> = MAX, See Note 2	26 45	26 45	мА

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup> All typical values are at  $V_{CC} = 5 V$ ,  $T_A = 25^{\circ}C$ . § Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

NOTE 2: One input at 4.5 V, all others at GND,

## switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = $25^{\circ}$ C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN TYP	MAX	UNIT
<sup>t</sup> PLH			$R_1 = 280 \Omega$ , $C_1 = 15 \rho F$	3.5	5,5	ns
tPHL		~	R <sub>L</sub> = 280 Ω, C <sub>L</sub> = 15 ρF	3.5	5.5	ns
<sup>t</sup> ₽LH	A or B			5		ns
<sup>t</sup> PHL			$R_{L} = 280 \ \Omega, \qquad C_{L} = 50 \ \rho F$	5		ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

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6-Dec-2006

## **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
JM38510/00401BCA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
JM38510/00401BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
JM38510/00401BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
JM38510/07301BCA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
JM38510/07301BCA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
JM38510/07301BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
JM38510/07301BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
JM38510/30301B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
JM38510/30301B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
JM38510/30301BCA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
JM38510/30301BCA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
JM38510/30301BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
JM38510/30301BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
JM38510/30301SCA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
JM38510/30301SCA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
JM38510/30301SDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
JM38510/30301SDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
SN5402J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SN5402J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SN54LS02J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SN54LS02J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SN54S02J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SN54S02J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SN7402N	ACTIVE	PDIP	Ν	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN7402N	ACTIVE	PDIP	Ν	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN7402N3	OBSOLETE	PDIP	Ν	14		TBD	Call TI	Call TI
SN7402N3	OBSOLETE	PDIP	Ν	14		TBD	Call TI	Call TI
SN7402NE4	ACTIVE	PDIP	Ν	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN7402NE4	ACTIVE	PDIP	Ν	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS02D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS02D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS02DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS02DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS02DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS02DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

# PACKAGE OPTION ADDENDUM

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6-Dec-2006

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Packag Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74LS02DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS02DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS02J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
SN74LS02J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
SN74LS02N	ACTIVE	PDIP	Ν	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS02N	ACTIVE	PDIP	Ν	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS02N3	OBSOLETE	PDIP	Ν	14		TBD	Call TI	Call TI
SN74LS02N3	OBSOLETE	PDIP	Ν	14		TBD	Call TI	Call TI
SN74LS02NE4	ACTIVE	PDIP	Ν	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS02NE4	ACTIVE	PDIP	Ν	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS02NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS02NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS02NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS02NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S02D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S02D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S02DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S02DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S02DR	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI
SN74S02DR	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI
SN74S02N	ACTIVE	PDIP	Ν	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74S02N	ACTIVE	PDIP	Ν	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74S02N3	OBSOLETE	PDIP	Ν	14		TBD	Call TI	Call TI
SN74S02N3	OBSOLETE	PDIP	Ν	14		TBD	Call TI	Call TI
SN74S02NE4	ACTIVE	PDIP	Ν	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74S02NE4	ACTIVE	PDIP	Ν	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SNJ5402J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ5402J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ5402W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
SNJ5402W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
SNJ54LS02FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SNJ54LS02FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LS02J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS02J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS02W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
SNJ54LS02W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
SNJ54S02FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54S02FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54S02J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54S02J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54S02W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
SNJ54S02W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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J (R-GDIP-T\*\*) 14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB



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## FK (S-CQCC-N\*\*)

## LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.
- E. Falls within JEDEC MS-004



# N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- $\triangle$  The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.

Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.

E. Reference JEDEC MS-012 variation AB.



## MECHANICAL DATA

## PLASTIC SMALL-OUTLINE PACKAGE

#### 0,51 0,35 ⊕0,25⊛ 1,27 8 14 0,15 NOM 5,60 8,20 5,00 7,40 $\bigcirc$ Gage Plane ₽ 0,25 7 1 1,05 0,55 0-10 Δ 0,15 0,05 Seating Plane — 2,00 MAX 0,10PINS \*\* 14 16 20 24 DIM 10,50 10,50 12,90 15,30 A MAX A MIN 9,90 9,90 12,30 14,70 4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.

NS (R-PDSO-G\*\*)

**14-PINS SHOWN** 

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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