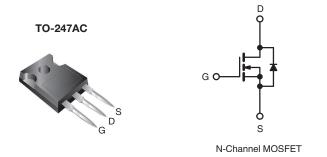


Power MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	1000				
$R_{DS(on)}(\Omega)$	V _{GS} = 10 V 2.0				
Q _g (Max.) (nC)	190				
Q _{gs} (nC)	23				
Q _{gd} (nC)	110				
Configuration	Single				



FEATURES

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Isolated Central Mounting Hole
- Fast Switching
- · Ease of Paralleling
- Simple Drive Requirements
- Compliant to RoHS Directive 2002/95/EC



DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-247AC for package preferred commercial-industrial applications where higher power levels preclude the use of TO-220AB devices. The TO-247AC is similar but superior to the earlier TO-218 package because its isolated mounting hole. It also provides greater creepage distances between pins to meet the requirements of most safety specifications.

ORDERING INFORMATION			
Package	TO-247AC		
Lead (Pb)-free	IRFPG50PbF		
Leau (FD)-iree	SiHFPG50-E3		
SnPb	IRFPG50		
SIFD	SiHFPG50		

PARAMETER	SYMBOL	LIMIT	UNIT		
Drain-Source Voltage		V _{DS}	1000	V	
Gate-Source Voltage		V_{GS}	± 20	7 V	
Continuous Drain Current	V_{GS} at 10 V $T_C = 25 ^{\circ}C$	I-	6.1		
Continuous Drain Guirent	$T_C = 100 ^{\circ}C$	I _D	3.9	A	
Pulsed Drain Current ^a		I _{DM}	24		
Linear Derating Factor		1.5	W/°C		
Single Pulse Avalanche Energy ^b	E _{AS}	800	mJ		
Repetitive Avalanche Current ^a	I _{AR}	6.0	Α		
Repetitive Avalanche Energy ^a		E _{AR}	19	mJ	
Maximum Power Dissipation	P_{D}	190	W		
Peak Diode Recovery dV/dtc	dV/dt	1.0	V/ns		
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to + 150	°C		
Soldering Recommendations (Peak Temperature) for 10 s			300 ^d		
Manustine Tanana	6-32 or M3 screw		10	lbf ⋅ in	
Mounting Torque	0-32 OF IVIS SCIEW		1.1	N⋅m	

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11). b. $V_{DD}=50~V$, starting $T_J=25~^{\circ}C$, L=40~mH, $R_g=25~\Omega$, $I_{AS}=6.1~A$ (see fig. 12). c. $I_{SD}\leq 6.1~A$, dl/dt $\leq 120~A/\mu s$, $V_{DD}\leq 600$, $T_J\leq 150~^{\circ}C$. d. 1.6 mm from case.

^{*} Pb containing terminations are not RoHS compliant, exemptions may apply



THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	TYP.	MAX.	UNIT	
Maximum Junction-to-Ambient	R _{thJA}	-	40		
Case-to-Sink, Flat, Greased Surface	R _{thCS}	0.24	-	°C/W	
Maximum Junction-to-Case (Drain)	R _{thJC}	-	0.65		

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static						l	
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0$	V, I _D = 250 μA	1000	-	-	V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Reference	to 25 °C, I _D = 1 mA	-	1.2	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V$	' _{GS} , I _D = 250 μA	2.0	-	4.0	V
Gate-Source Leakage	I _{GSS}	V _G	_S = ± 20 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}		000 V, V _{GS} = 0 V	-	-	100	μА
20.0 date 10.1age 2.a 0ao	.033	$V_{DS} = 800 \text{ V}, \text{ V}$	/ _{GS} = 0 V, T _J = 125 °C	-	-	500	μΑ
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	$I_D = 3.6 A^b$	-	-	2.0	Ω
Forward Transconductance	9fs	$V_{DS} = 10$	00 V, I _D = 3.6 A ^b	5.4	-	-	S
Dynamic							
Input Capacitance	C_{iss}	V	$t_{GS} = 0 \text{ V},$	-	2800	-	
Output Capacitance	C _{oss}	V	os = 25 V,	-	250	-	pF
Reverse Transfer Capacitance	C_{rss}	f = 1.0 MHz, see fig. 5		-	84	-	
Total Gate Charge	Qg			-	-	190	nC
Gate-Source Charge	Q _{gs}	V _{GS} = 10 V	$I_D = 6.1 \text{ A}, V_{DS} = 400 \text{ V},$ see fig. 6 and 13 ^b	-	-	23	
Gate-Drain Charge	Q _{gd}	see lig. 6 and 15		-	-	110	
Turn-On Delay Time	t _{d(on)}	$V_{DD} = 500 \text{ V, } I_D = 6.1 \text{ A,}$ $R_g = 6.2 \ \Omega, \ R_D = 81 \ \Omega, \ \text{see fig. } 10^b$		-	19	-	ns
Rise Time	t _r			-	35	-	
Turn-Off Delay Time	t _{d(off)}			-	130	-	
Fall Time	t _f			-	36	-	
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") from		-	5.0	-	-11
Internal Source Inductance	L _S	package and ce die contact	package and center of		13	-	- nH
Drain-Source Body Diode Characteristic	s	·					
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	6.1	A
Pulsed Diode Forward Current ^a	I _{SM}			-	-	24	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I ₅	T _J = 25 °C, I _S = 6.1 A, V _{GS} = 0 V ^b		-	1.8	V
Body Diode Reverse Recovery Time	t _{rr}	T 05 °C 1	C 1 A d1/d+ 100 A/b	-	630	950	ns
Body Diode Reverse Recovery Charge	Q _{rr}	$T_J = 25 ^{\circ}\text{C}, I_F = 6.1 \text{A}, \text{dI/dt} = 100 \text{A/}\mu\text{s}^b$		-	3.5	5.3	μC
Forward Turn-On Time	t _{on}	Intrinsic turn	-on time is negligible (turn	on is dor	minated b	y L _S and	L _D)

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width $\leq 300~\mu s;$ duty cycle $\leq 2~\%.$



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

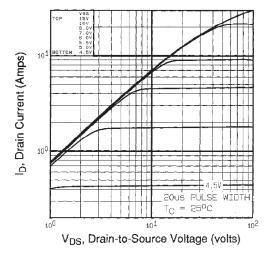


Fig. 1 - Typical Output Characteristics, T_C = 25 °C

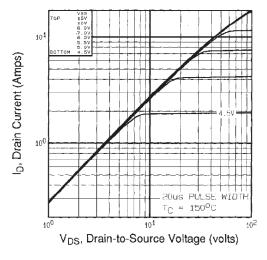
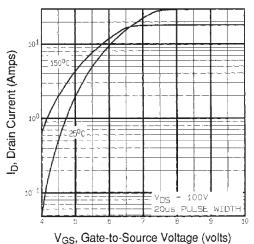


Fig. 2 - Typical Output Characteristics, T_C = 150 °C



VGS, date to bourse voltage (volta)

Fig. 3 - Typical Transfer Characteristics

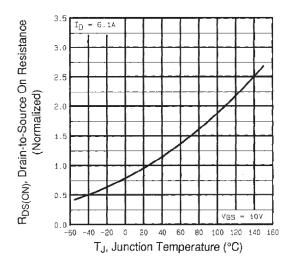


Fig. 4 - Normalized On-Resistance vs. Temperature



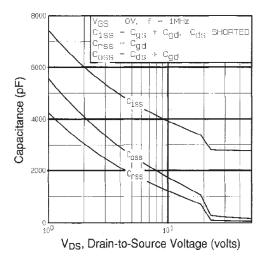


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

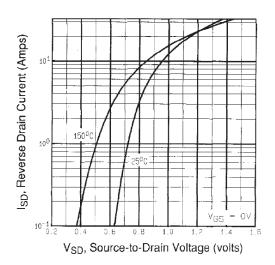


Fig. 7 - Typical Source-Drain Diode Forward Voltage

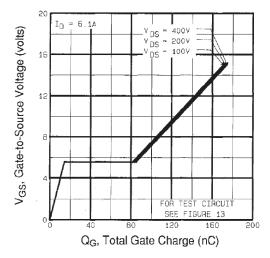


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

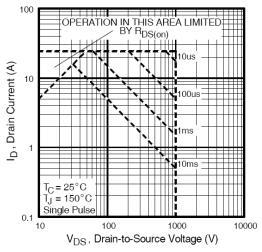


Fig. 8 - Maximum Safe Operating Area





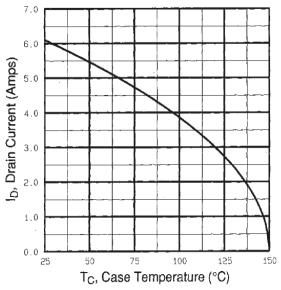


Fig. 9 - Maximum Drain Current vs. Case Temperature

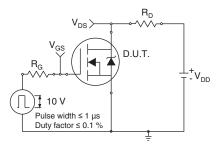


Fig. 10a - Switching Time Test Circuit

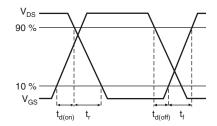


Fig. 10b - Switching Time Waveforms

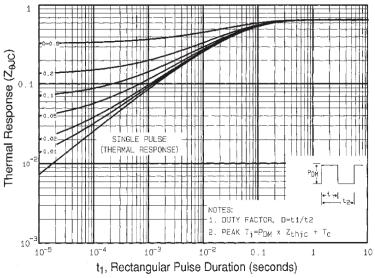
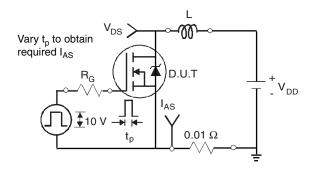


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case





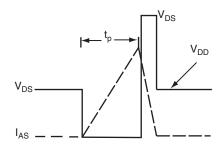


Fig. 12a - Unclamped Inductive Test Circuit

Fig. 12b - Unclamped Inductive Waveforms

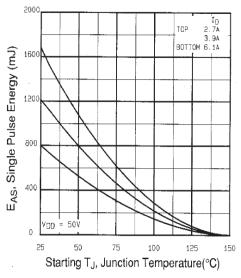


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

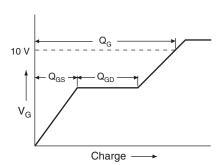


Fig. 13a - Basic Gate Charge Waveform

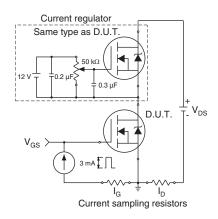
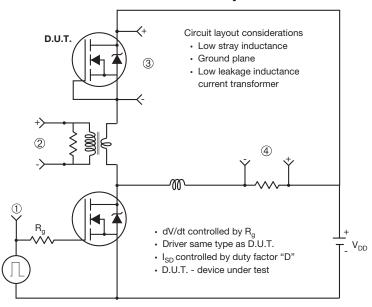


Fig. 13b - Gate Charge Test Circuit



Peak Diode Recovery dV/dt Test Circuit



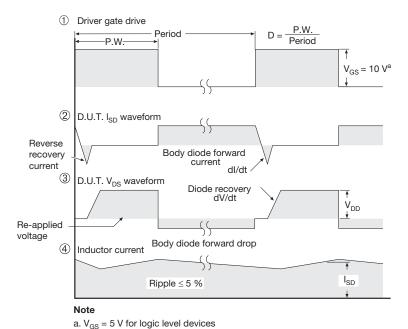
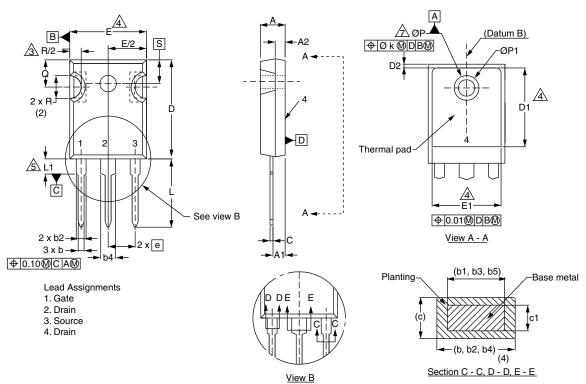


Fig. 14 - For N-Channel

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TO-247AC (High Voltage)



	MILLIMETERS		INC	HES
DIM.	MIN.	MAX.	MIN.	MAX.
Α	4.58	5.31	0.180	0.209
A1	2.21	2.59	0.087	0.102
A2	1.17	2.49	0.046	0.098
b	0.99	1.40	0.039	0.055
b1	0.99	1.35	0.039	0.053
b2	1.53	2.39	0.060	0.094
b3	1.65	2.37	0.065	0.093
b4	2.42	3.43	0.095	0.135
b5	2.59	3.38	0.102	0.133
С	0.38	0.86	0.015	0.034
c1	0.38	0.76	0.015	0.030
D	19.71	20.82	0.776	0.820
D1	13.08	-	0.515	-

	MILLIMETERS		INC	HES	
DIM.	MIN.	MAX.	MIN.	MAX.	
D2	0.51	1.30	0.020	0.051	
E	15.29	15.87	0.602	0.625	
E1	13.72	ı	0.540	ı	
е	5.46	BSC	0.215 BSC		
Øk	0.2	254	0.010		
L	14.20	16.25	0.559	0.640	
L1	3.71	4.29	0.146	0.169	
N	7.62	7.62 BSC		0.300 BSC	
ØΡ	3.51	3.66	0.138	0.144	
Ø P1	-	7.39	-	0.291	
Q	5.31	5.69	0.209	0.224	
R	4.52	5.49	0.178	0.216	
S	5.51 BSC		0.217 BSC		
0.01200					

ECN: X13-0103-Rev. D, 01-Jul-13

DWG: 5971

Notes

- 1. Dimensioning and tolerancing per ASME Y14.5M-1994.
- 2. Contour of slot optional.
- 3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body.
- 4. Thermal pad contour optional with dimensions D1 and E1.
 5. Lead finish uncontrolled in L1.
- 6. Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154").
- 7. Outline conforms to JEDEC outline TO-247 with exception of dimension c.
- 8. Xian and Mingxin actually photo.





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