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FEATURES

■ Avalanche Rugged Technology

■ Rugged Gate Oxide Technology

■ Lower Input Capacitance

■ Improved Gate Charge

■ Extended Safe Operating Area

■ 175°C Operating Temperature

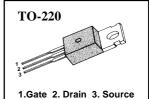
■ Lower Leakage Current : 10 μ A (Max.) @ $V_{DS} = 100V$

■ Lower $R_{DS(ON)}$: 0.092 $\Omega(Typ.)$

 $BV_{DSS} = 100 V$

 $R_{DS(on)} = 0.11 \Omega$

 $I_D = 14 A$



Absolute Maximum Ratings

Symbol	Characteristic		Value	Units	
V _{DSS}	Drain-to-Source Voltage	100	V		
,	Continuous Drain Current (T _C =25°C)		14		
I _D	Continuous Drain Current (T _c =100 °C)		9.9	Α	
I _{DM}	Drain Current-Pulsed	0	56	Α	
V _{GS}	Gate-to-Source Voltage	<u>+</u> 2 0	V		
E _{AS}	Single Pulsed Avalanche Energy	2	261	mJ	
I _{AR}	Avalanche Current	0	14	Α	
E _{AR}	Repetitive Avalanche Energy	0	5.5	mJ	
dv/dt	Peak Diode Recovery dv/dt	3	6.5	V/ns	
Ь	Total Power Dissipation (T _C =25°C)		55	W	
P_{D}	Linear Derating Factor		0.36	W/°C	
	Operating Junction and		FF to 147F		
T_J , T_STG	Storage Temperature Range		- 55 to +175	°C	
	Maximum Lead Temp. for Soldering		200		
T _L	Purposes, 1/8" from case for 5-seco	nds	300		

Thermal Resistance

Symbol	Characteristic	Тур.	Max.	Units
R _{θJC}	Junction-to-Case	1	2.74	
R _{ecs}	Case-to-Sink	0.5	1	°C/W
R _{θJA}	Junction-to-Ambient	-	62.5	

Electrical Characteristics (T_C=25°C unless otherwise specified)

Symbol	Characteristic	Min.	Тур.	Max.	Units	Test Condition		
BV _{DSS}	Drain-Source Breakdown Voltage	100	1	1	V	$V_{GS} = 0V, I_{D} = 250 \mu\text{A}$		
Δ BV/ Δ T $_{ m J}$	Breakdown Voltage Temp. Coeff.		0.11	1	V/°C	I _D =250 μA See Fig 7		
$V_{GS(th)}$	Gate Threshold Voltage	2.0	-	4.0	V	$V_{DS} = 5V, I_{D} = 250 \mu A$		
l	Gate-Source Leakage, Forward		-	100	nA	V _{GS} =20V		
I _{GSS}	Gate-Source Leakage, Reverse			-100	ш	V _{GS} =-20V		
	Drain to Source Lackage Current			10	μА	V _{DS} =100V		
I _{DSS}	Drain-to-Source Leakage Current			100		V_{DS} =80V, T_{C} =150°C		
ь	Static Drain-Source			0.44	Ω	V _{cc} =10V.I _c =7A 4		
R _{DS(on)}	On-State Resistance		-	- 0.11	0.11	0.11	52	$V_{GS}=10V,I_{D}=7A$
g_{fs}	Forward Transconductance		10.25		Ω	V_{DS} =40V, I_{D} =7A 4		
C _{iss}	Input Capacitance		610	790		$V_{GS}=0V, V_{DS}=25V, f=1MHz$		
C _{oss}	Output Capacitance		150	175	pF	See Fig 5		
C_{rss}	Reverse Transfer Capacitance		62	72		See Fig 5		
$t_{d(on)}$	Turn-On Delay Time		13	40		V _{DD} =50V,I _D =14A,		
t _r	Rise Time		14	40	nc	$R_{G}=12\Omega$		
$t_{d(off)}$	Turn-Off Delay Time		55	110	ns	See Fig 13 46		
t _f	Fall Time		36	80		See Fig 13 90		
Q_g	Total Gate Charge		27	36		V_{DS} =80V, V_{GS} =10V,		
Q_gs	Gate-Source Charge		4.5		nC	I _D =14A		
Q_gd	Gate-Drain("Miller") Charge		12.8			See Fig 6 & Fig 12 ^④ ⑤		

Source-Drain Diode Ratings and Characteristics

Symbol	Characteristic	Min.	Тур.	Max.	Units	Test Condition
I _S	Continuous Source Current			14	Α	Integral reverse pn-diode
I _{SM}	Pulsed-Source Current ①			56	A	in the MOSFET
V _{SD}	Diode Forward Voltage 4			1.5	V	$T_J=25$ °C, $I_S=14A$, $V_{GS}=0V$
t _{rr}	Reverse Recovery Time		109	-	ns	T _J =25°C,I _F =14A
Q _{rr}	Reverse Recovery Charge		0.41		¥ìC	di _F /dt=100A/μs

- Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature
- 2 L=2mH, I_{AS} =14A, V_{DD} =25V, R_{G} =27 Ω , Starting T_{J} =25 $^{\circ}$ C
- (3) $I_{SD} \le 14A$, di/dt $\le 350A/\mu s$, $V_{DD} \le BV_{DSS}$, Starting $T_J = 25^{\circ}C$ (4) Pulse Test : Pulse Width = 250 μs , Duty Cycle $\le 2\%$
- **(5)** Essentially Independent of Operating Temperature



Fig 1. Output Characteristics

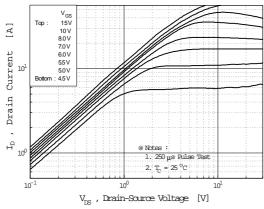


Fig 2. Transfer Characteristics

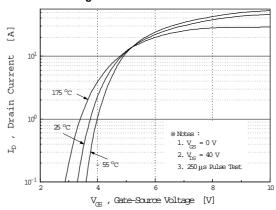


Fig 3. On-Resistance vs. Drain Current

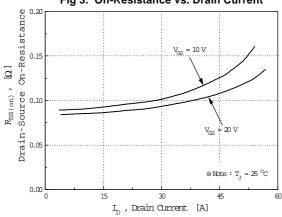


Fig 4. Source-Drain Diode Forward Voltage

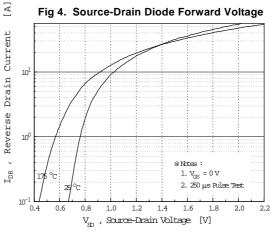


Fig 5. Capacitance vs. Drain-Source Voltage

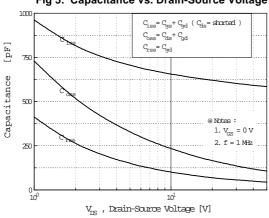
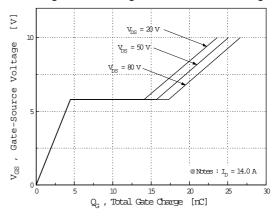
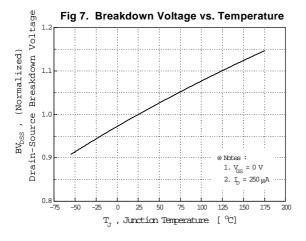
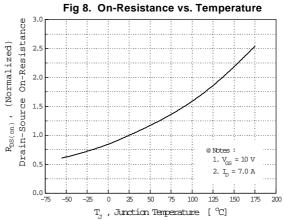


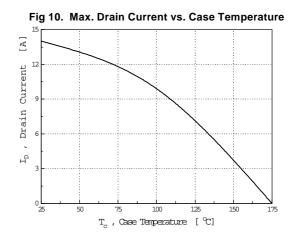
Fig 6. Gate Charge vs. Gate-Source Voltage











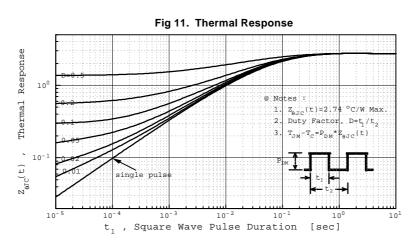




Fig 12. Gate Charge Test Circuit & Waveform

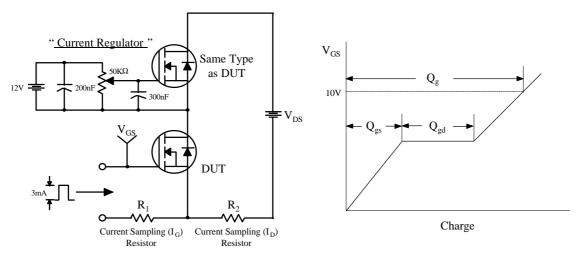


Fig 13. Resistive Switching Test Circuit & Waveforms

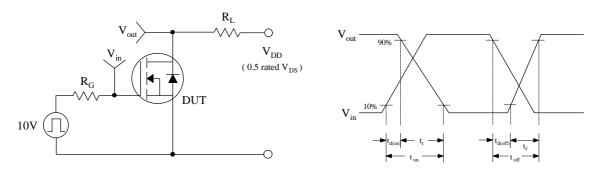


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

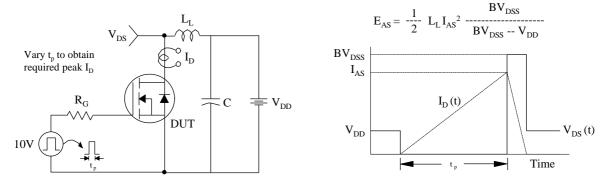
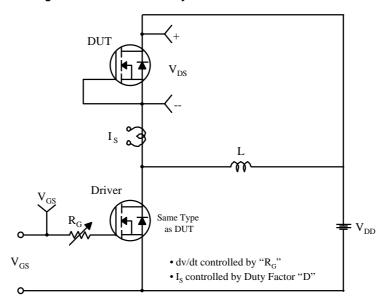
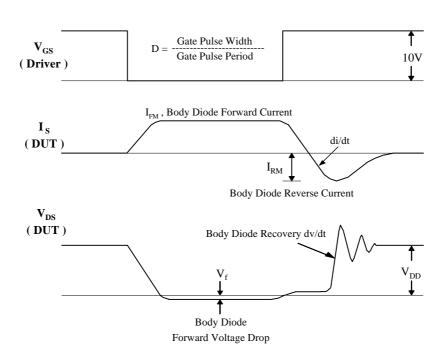


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms







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