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Kind regards,

Team Nexperia

PSMN2R0-60PS

N-channel 60 V 2.2 mΩ standard level MOSFET in TO-220

4 October 2012

Product data sheet

1. Product profile

1.1 General description

Standard level N-channel MOSFET in a TO-220 package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for standard level gate drive sources

1.3 Applications

- DC-to-DC converters
- Load switching
- Motor control
- Server power supplies

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C		-	-	60	V
I _D	drain current	T _{mb} = 25 °C; V _{GS} = 10 V; Fig. 1	[1]	-	-	120	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 2		-	-	338	W
T _j	junction temperature			-55	-	175	°C
Static characteristics							
R _{DS(on)}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; Fig. 12	[2]	-	1.8	2.2	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 100 °C; Fig. 12 ; Fig. 13		-	3	3.5	mΩ
Dynamic characteristics							
Q _{GD}	gate-drain charge	V _{GS} = 10 V; I _D = 75 A; V _{DS} = 30 V; Fig. 14 ; Fig. 15		-	32	45	nC
Q _{G(tot)}	total gate charge			-	137	192	nC

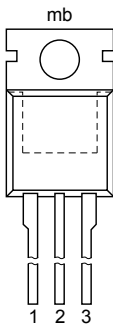
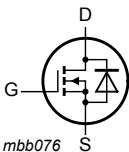


Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ °C}$; $I_D = 120\text{ A}$; $V_{\text{sup}} \leq 60\text{ V}$; $R_{GS} = 50\text{ }\Omega$; Unclamped	-	-	913	mJ

- [1] Continuous current limited by package
- [2] Measured 3 mm from package.

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p style="text-align: center;">TO-220AB (SOT78)</p>	
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN2R0-60PS	TO-220AB	plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB	SOT78

4. Marking

Table 4. Marking codes

Type number	Marking code
PSMN2R0-60PS	PSMN2R0-60PS

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$		-	60	V
V_{DGR}	drain-gate voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}; R_{GS} = 20\text{ k}\Omega$		-	60	V
V_{GS}	gate-source voltage			-20	20	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 100\text{ °C}; \text{Fig. 1}$	[1]	-	120	A
		$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C}; \text{Fig. 1}$	[1]	-	120	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}; T_{mb} = 25\text{ °C}; \text{Fig. 3}$		-	1135	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}; \text{Fig. 2}$		-	338	W
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
Source-drain diode						
I_S	source current	$T_{mb} = 25\text{ °C}$	[1]	-	120	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}; T_{mb} = 25\text{ °C}$		-	1135	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}; T_{j(\text{init})} = 25\text{ °C}; I_D = 120\text{ A}; V_{sup} \leq 60\text{ V}; R_{GS} = 50\text{ }\Omega; \text{Unclamped}$		-	913	mJ

[1] Continuous current limited by package

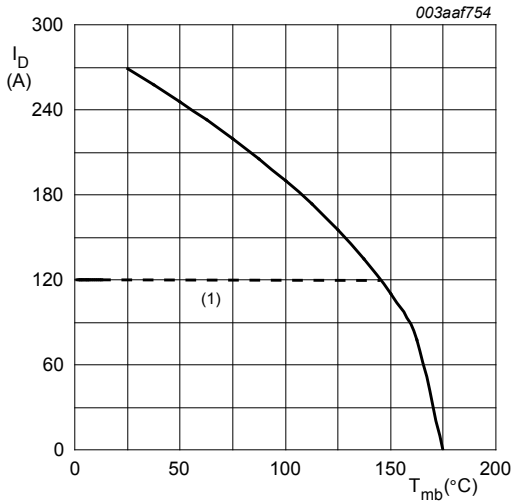


Fig. 1. Continuous drain current as a function of mounting base temperature.

$V_{GS} \geq 10$ V; (1) Capped at 120 A due to package

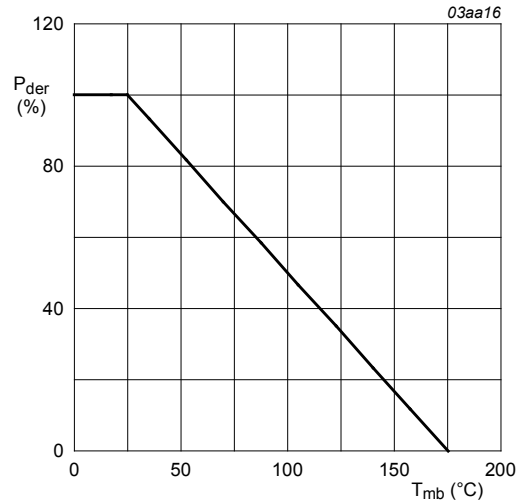


Fig. 2. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

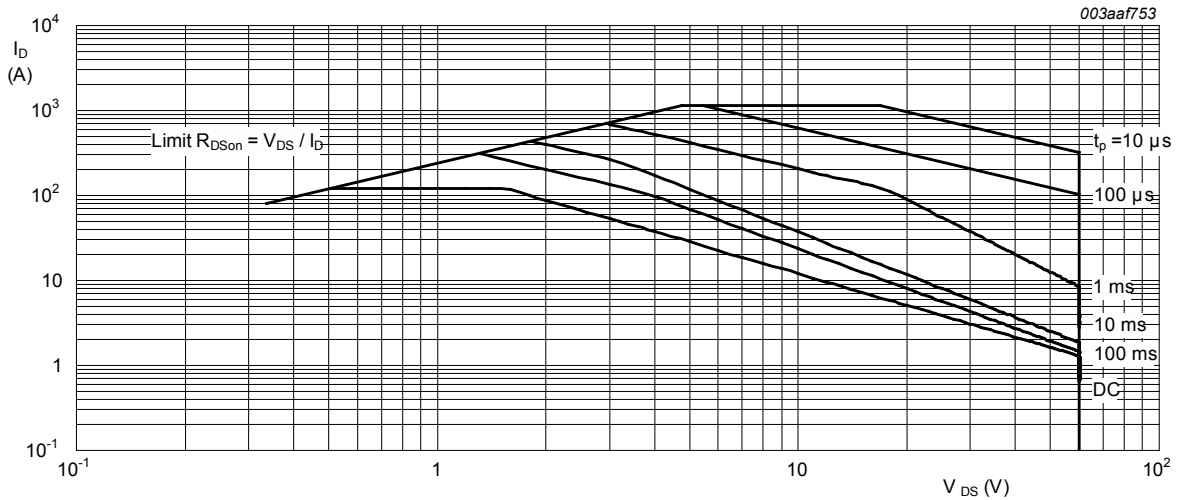


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25$ °C; I_{DM} is a single pulse; Capped at 120 A due to package

6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4	-	0.22	0.44	K/W

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	Vertical in free air	-	60	-	K/W

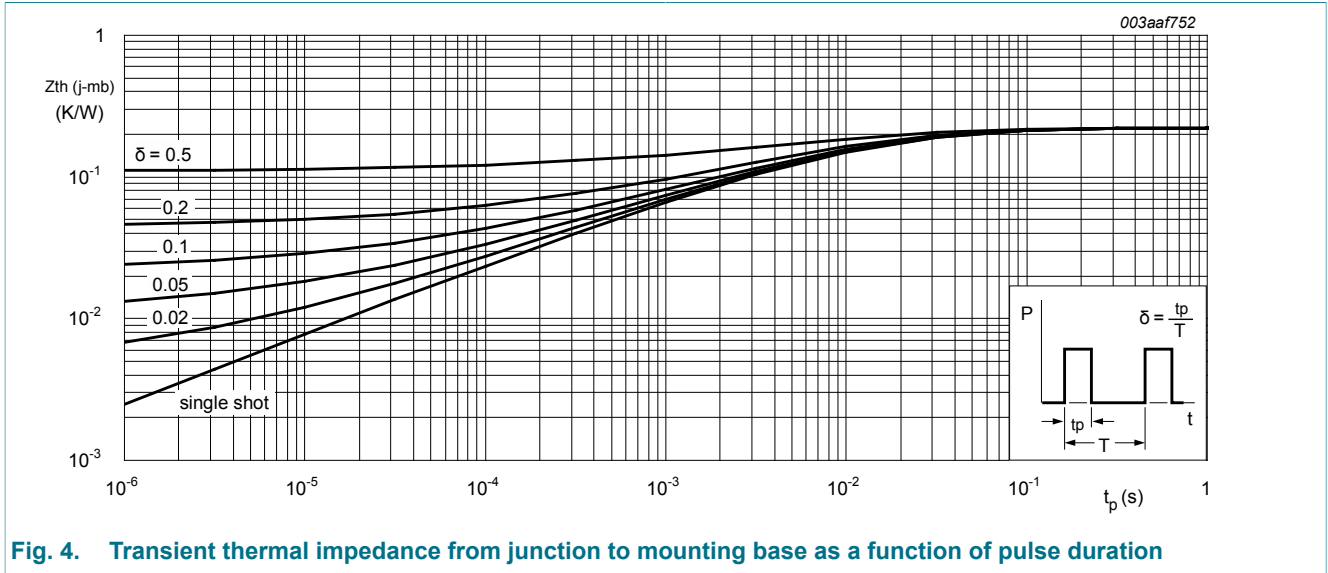


Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

7. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	54	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	60	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C;$ Fig. 10	1	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C;$ Fig. 11; Fig. 10	2	3	4	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C;$ Fig. 10	-	-	4.6	V
I_{DSS}	drain leakage current	$V_{DS} = 60 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.03	10	μA
		$V_{DS} = 60 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ C$	-	-	500	μA
I_{GSS}	gate leakage current	$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	-	100	nA
		$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	-	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C;$ Fig. 12	[1]	1.8	2.2	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ C;$ Fig. 12; Fig. 13	-	4.3	5.1	mΩ

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 100\text{ °C};$ Fig. 12 ; Fig. 13	-	3	3.5	mΩ
R_G	gate resistance	$f = 1\text{ MHz}$	0.45	0.9	1.8	Ω
Dynamic characteristics						
$Q_{G(\text{tot})}$	total gate charge	$I_D = 75\text{ A}; V_{DS} = 30\text{ V}; V_{GS} = 10\text{ V};$ Fig. 14 ; Fig. 15	-	137	192	nC
		$I_D = 0\text{ A}; V_{DS} = 0\text{ V}; V_{GS} = 10\text{ V};$ Fig. 14 ; Fig. 15	-	129	181	nC
Q_{GS}	gate-source charge	$I_D = 75\text{ A}; V_{DS} = 30\text{ V}; V_{GS} = 10\text{ V}$	-	48	68	nC
$Q_{GS(\text{th})}$	pre-threshold gate-source charge	$I_D = 75\text{ A}; V_{DS} = 30\text{ V}; V_{GS} = 10\text{ V};$ Fig. 14 ; Fig. 15	-	29	-	nC
$Q_{GS(\text{th-pl})}$	post-threshold gate-source charge		-	19	-	nC
Q_{GD}	gate-drain charge		-	32	45	nC
$V_{GS(\text{pl})}$	gate-source plateau voltage	$V_{DS} = 30\text{ V};$ Fig. 14 ; Fig. 15	-	5.7	-	V
C_{iss}	input capacitance	$V_{DS} = 30\text{ V}; V_{GS} = 0\text{ V}; f = 1\text{ MHz};$ $T_j = 25\text{ °C};$ Fig. 16	-	9997	13500	pF
C_{oss}	output capacitance		-	1210	1640	pF
C_{rss}	reverse transfer capacitance		-	594	835	pF
$t_{d(\text{on})}$	turn-on delay time	$V_{DS} = 30\text{ V}; R_L = 0.4\text{ Ω}; V_{GS} = 10\text{ V};$ $R_{G(\text{ext})} = 4.7\text{ Ω}; I_D = 75\text{ A}$	-	42	63	ns
t_r	rise time		-	56	84	ns
$t_{d(\text{off})}$	turn-off delay time		-	115	173	ns
t_f	fall time		-	49	74	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ °C};$ Fig. 17	-	0.8	1.2	V
t_{rr}	reverse recovery time	$I_S = 25\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$ $V_{DS} = 30\text{ V}$	-	57	75	ns
Q_r	recovered charge	$I_S = 25\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$ $V_{DS} = 30\text{ V}$	-	80	104	nC

[1] Measured 3 mm from package.

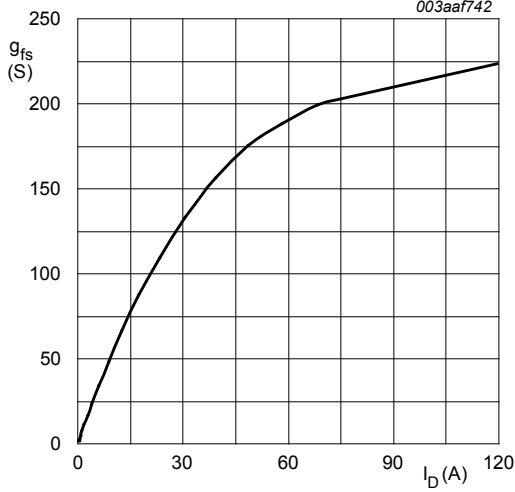


Fig. 5. Forward transconductance as a function of drain current; typical values

$T_j = 25\text{ °C}; V_{DS} = 30\text{ V}$

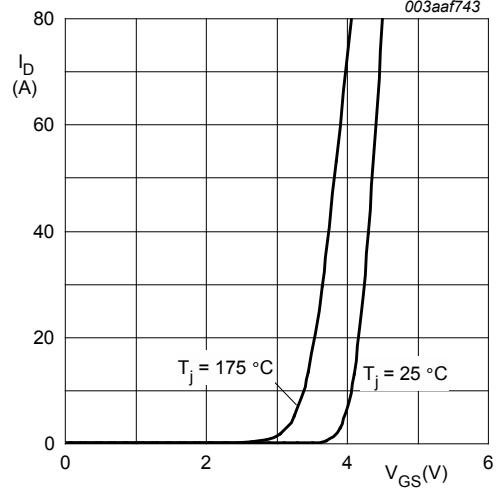


Fig. 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values

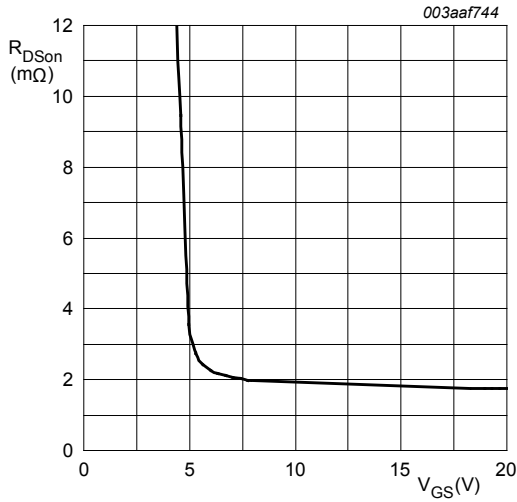


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25\text{ °C}; I_D = 25\text{ A}$

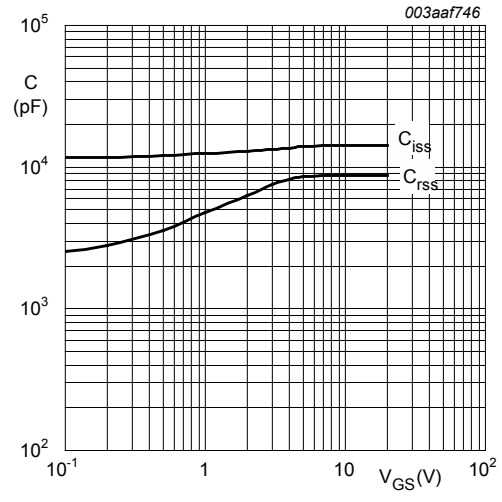


Fig. 8. Input and reverse transfer capacitances as a function of gate-source voltage, typical values

$V_{DS} = 0\text{ V}; f = 1\text{ MHz}$

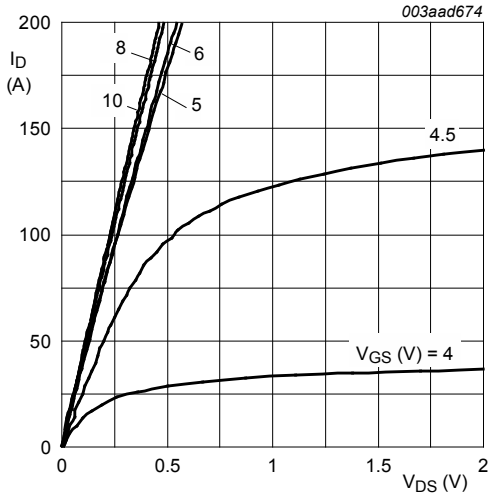


Fig. 9. Output characteristics: drain current as a function of drain-source voltage; typical values

$T_j = 25^\circ C$

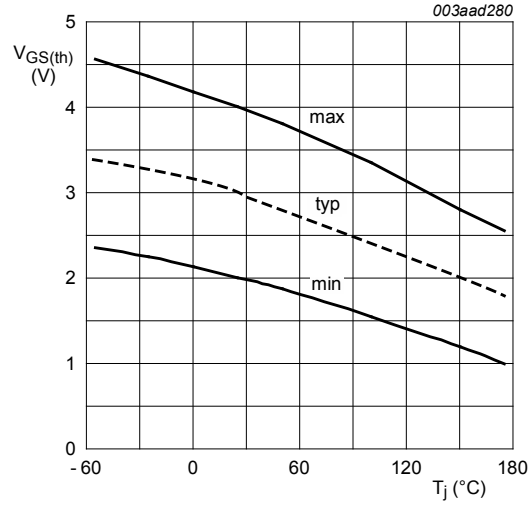


Fig. 10. Gate-source threshold voltage as a function of junction temperature

$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

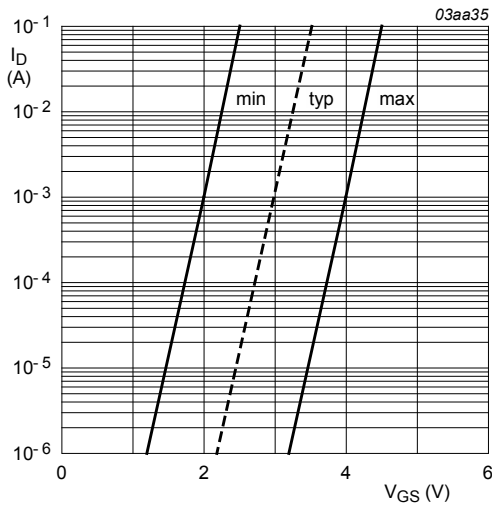


Fig. 11. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25^\circ C; V_{DS} = 5V$

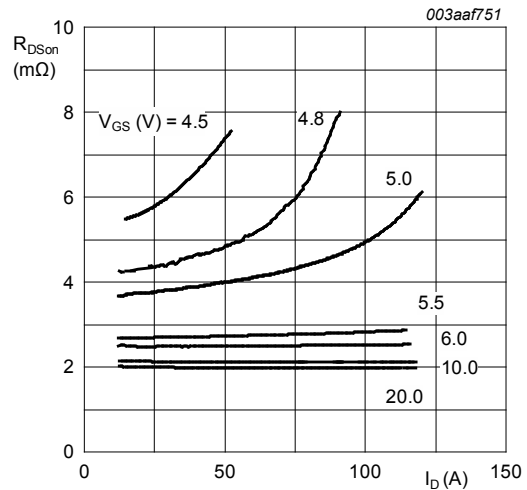


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

$T_j = 25^\circ C$

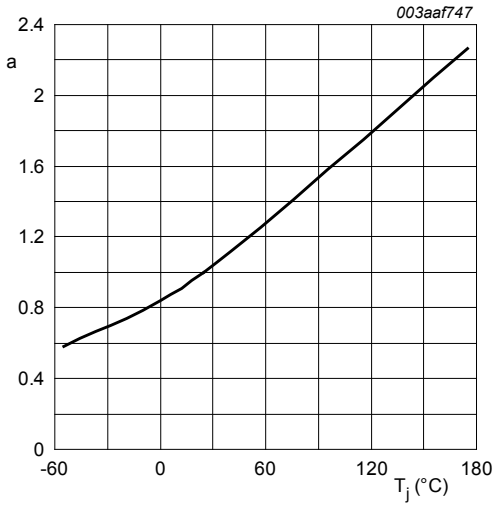


Fig. 13. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25\text{ °C}; I_D = 25\text{ A}$

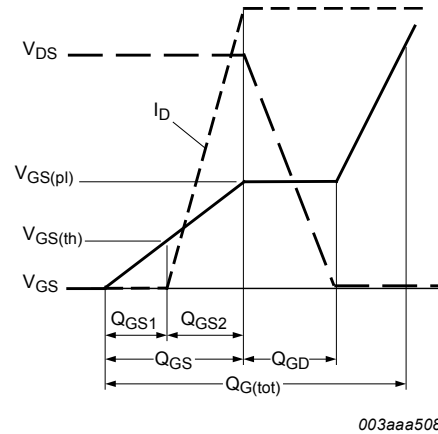


Fig. 14. Gate charge waveform definitions

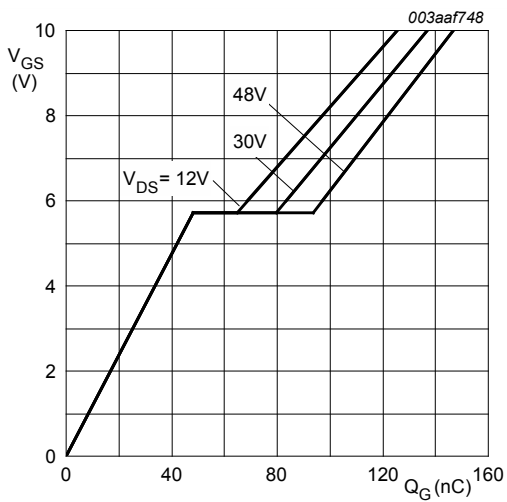


Fig. 15. Gate-source voltage as a function of gate charge; typical values

$T_j = 25\text{ °C}; I_D = 75\text{ A}$

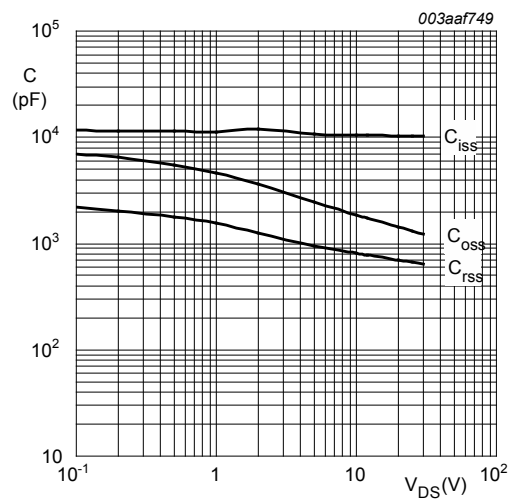


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

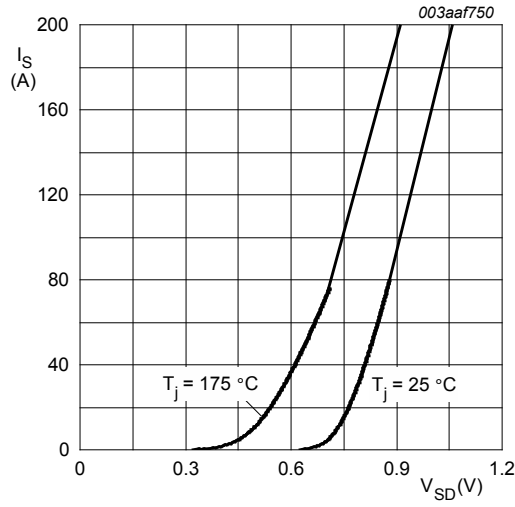


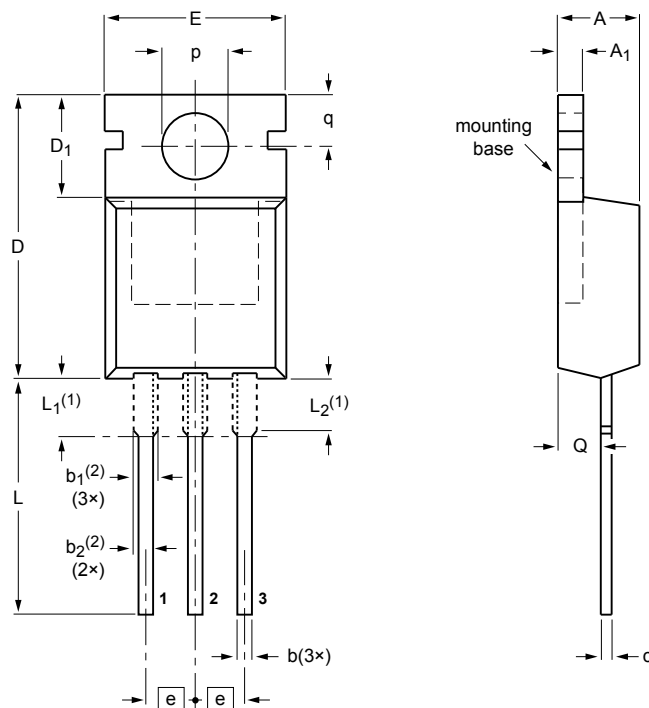
Fig. 17. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

$$V_{GS} = 0\text{ V}$$

8. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB

SOT78



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b	b ₁ (2)	b ₂ (2)	c	D	D ₁	E	e	L	L ₁ (1)	L ₂ (1) max.	p	q	Q
mm	4.7 4.1	1.40 1.25	0.9 0.6	1.6 1.0	1.3 1.0	0.7 0.4	16.0 15.2	6.6 5.9	10.3 9.7	2.54	15.0 12.8	3.30 2.79	3.0	3.8 3.5	3.0 2.7	2.6 2.2

Notes

- 1. Lead shoulder designs may vary.
- 2. Dimension includes excess dambar.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT78		3-lead TO-220AB	SC-46		08-04-23 08-06-13

Fig. 18. Package outline TO-220AB (SOT78)

9. Legal information

9.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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