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February 2015

# MMBTA56 / PZTA56 PNP General-Purpose Amplifier

# **Description**

This device is designed for general-purpose amplifier applications at collector currents to 300 mA. Sourced from process 73.

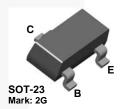


Figure 1. MMBTA56 Device Package

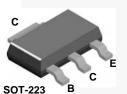


Figure 2. PZTA56 Device Package

# **Ordering Information**

Part Number Marking		Package	Packing Method
MMBTA56	2G	SOT-23 3L	Tape and Reel
PZTA56	A56	SOT-223 4L	Tape and Reel

# **Absolute Maximum Ratings**(1),(2)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at  $T_A = 25^{\circ}\text{C}$  unless otherwise noted.

Symbol	Parameter	Value	Unit
V <sub>CES</sub>	Collector-Emitter Voltage	-80	V
V <sub>CBO</sub>	Collector-Base Voltage	-80	V
V <sub>EBO</sub>	Emitter-Base Voltage	-4.0	V
I <sub>C</sub>	Collector Current - Continuous	-500	mA
$T_{J}$ , $T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

#### Notes:

- 1. These ratings are based on a maximum junction temperature of 150°C.
- 2. These are steady-state limits. Fairchild Semiconductor should be consulted on applications involving pulsed or low-duty-cycle operations.

# **Thermal Characteristics**

Values are at  $T_A = 25$ °C unless otherwise noted.

Symbol	Parameter	Ma	Unit	
	Farameter	MMBTA56 <sup>(3)</sup>	PZTA56 <sup>(4)</sup>	Onit
D	Total Device Dissipation	350	1000	mW
P <sub>D</sub>	Derate Above 25°C	2.8	8.0	mW/°C
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	357	125	°C/W

## Notes:

- 3. Device mounted on FR-4 PCB 36mm × 18mm × 1.5mm; mounting pad for the collector lead minimum 6cm<sup>2</sup>.
- 4. PCB size: FR-4, 76 mm x 114 mm x 1.57 mm (3.0 inch x 4.5 inch x 0.062 inch) with minimum land pattern size.

# **Electrical Characteristics**

Values are at  $T_A = 25$ °C unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Max.	Unit
V <sub>(BR)CEO</sub>	Collector-Emitter Breakdown Voltage <sup>(5)</sup>	I <sub>C</sub> = -1.0 mA, I <sub>B</sub> = 0	-80		V
V <sub>(BR)CBO</sub>	Collector-Base Breakdown Voltage	$I_C = -100 \mu A, I_E = 0$	-60		V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	$I_E = -100  \mu A,  I_C = 0$	-4.0		V
I <sub>CEO</sub>	Collector Cut-Off Current	$V_{CE} = -60 \text{ V}, I_{B} = 0$		-0.1	μΑ
I <sub>CBO</sub>	Collector Cut-Off Current	$V_{CB} = -80 \text{ V}, I_{E} = 0$		-0.1	μΑ
h <sub>FE</sub>	DC Current Gain	$I_C = -10 \text{ mA}, V_{CE} = -1.0 \text{ V}$	100		
		$I_C = -100 \text{ mA}, V_{CE} = -1.0 \text{ V}$	100		
V <sub>CE</sub> (sat)	Collector-Emitter Saturation Voltage	I <sub>C</sub> = -100 mA, I <sub>B</sub> = -10 mA		-0.25	V
V <sub>BE</sub> (on)	Base-Emitter On Voltage	$I_C = -100 \text{ mA}, V_{CE} = -1.0 \text{ V}$		-1.2	V
f <sub>T</sub>	Current Gain - Bandwidth Product	I <sub>C</sub> = -100 mA, V <sub>CE</sub> = -1.0 V, f = 100 MHz	50		MHz

# Note:

5. Pulse test: pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2.0%.

# **Typical Performance Characteristics**

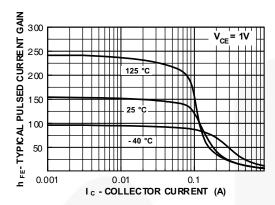


Figure 3. Typical Pulsed Current Gain vs. Collector Current

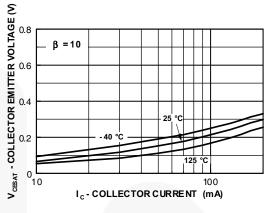


Figure 4. Collector-Emitter Saturation Voltage vs.
Collector Current

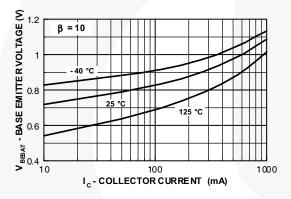


Figure 5. Base-Emitter Saturation Voltage vs.
Collector Current

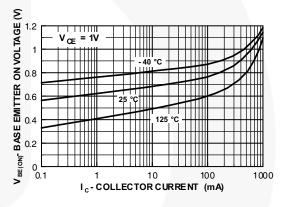


Figure 6. Base-Emitter On Voltage vs.
Collector Current

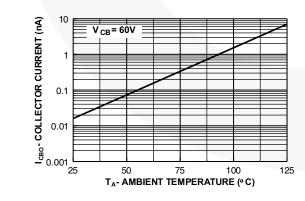


Figure 7. Collector Cut-Off Current vs.
Ambient Temperature

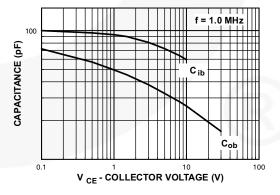


Figure 8. Input and Output Capacitance vs. Reverse Voltage

# **Typical Performance Characteristics** (Continued)

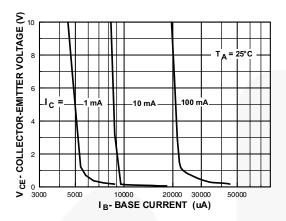


Figure 9. Collector Saturation Region

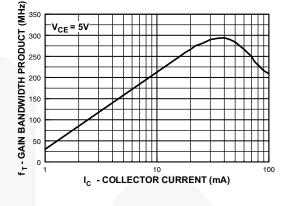


Figure 10. Gain Bandwidth Product vs. Collector Current

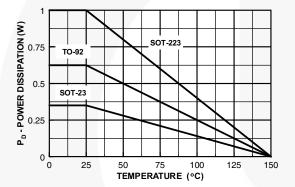
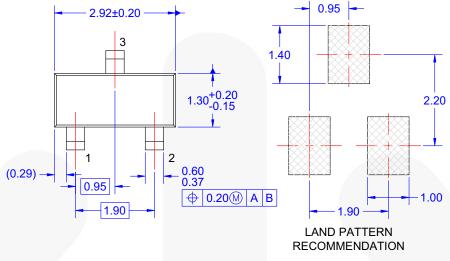
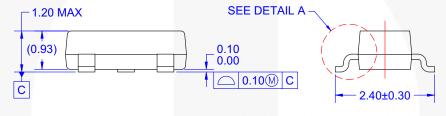
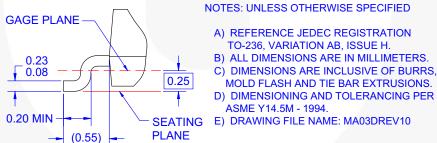


Figure 11. Power Dissipation vs.
Ambient Temperature

# Physical Dimensions



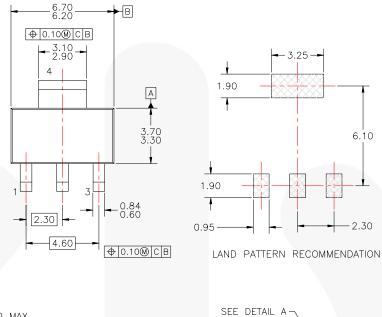


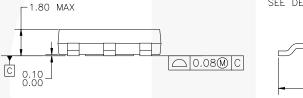


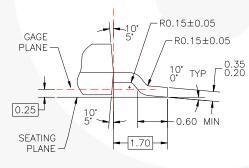
DETAIL A
SCALE: 2X

Figure 12. 3-LEAD, SOT23, JEDEC TO-236, LOW PROFILE

# Physical Dimensions (Continued)







DETAIL A

NOTES: UNLESS OTHERWISE SPECIFIED

7.30 6.70

- DRAWING BASED ON JEDEC
  REGISTRATION TO-261, VARIATION AA.
  DIMENSIONS ARE INCLUSIVE OF BURRS,
  MOLD FLASH AND TIE BAR EXTRUSIONS.
  ALL DIMENSIONS ARE IN MILLIMETERS.
  DRAWING CONFORMS TO ASME
  Y14.5M-1994.
  LANDPATTERN NAME:
  S0T230P700X180-4BN
  DRAWING FILENAME: MKT-MA04AREV2
- E)

Figure 13. MOLDED PACKAGING, SOT-223, 4-LEAD





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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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